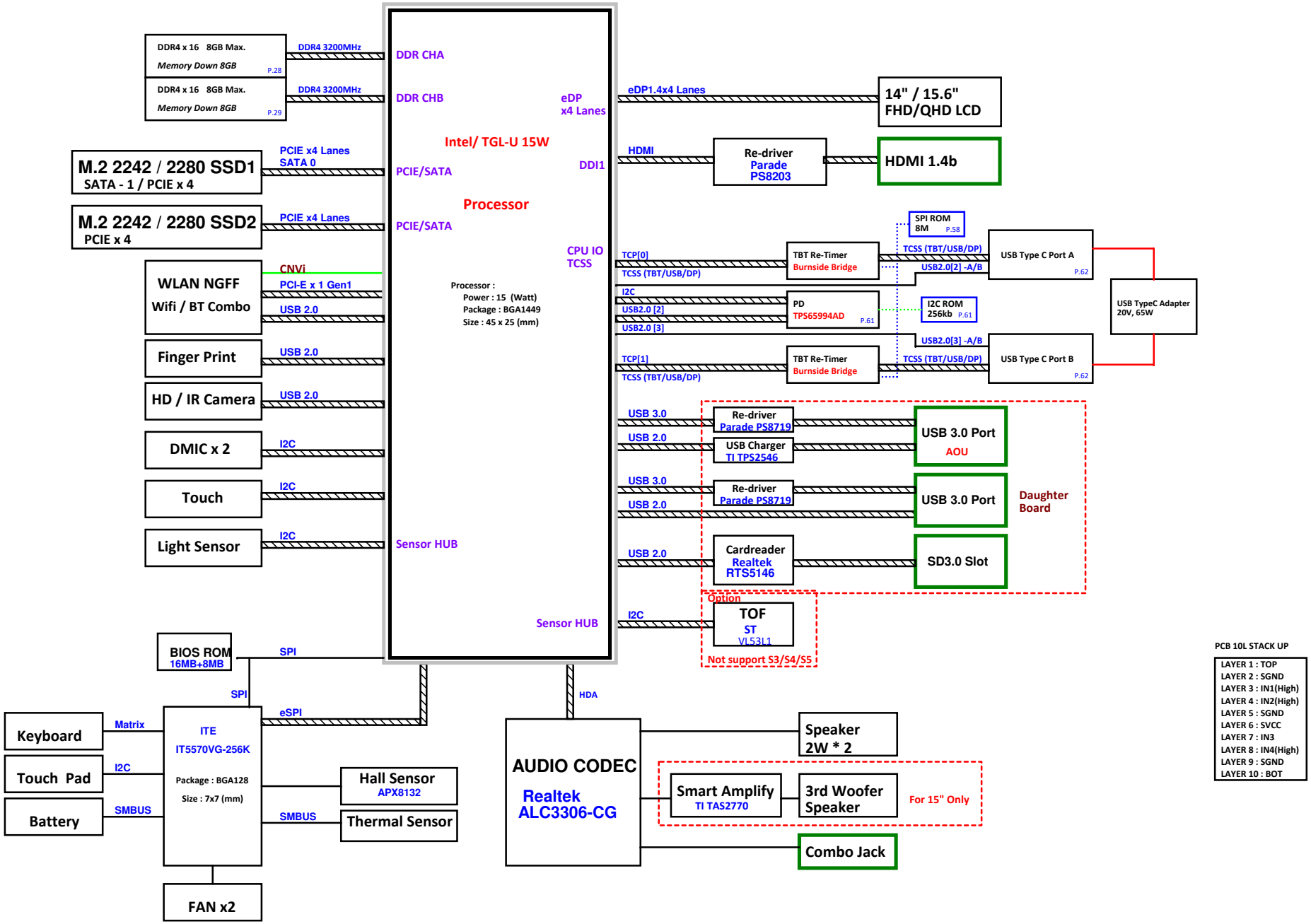
S750-14/15 Intel TGL-U Block Diagram



PCB 10L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : SVCC
LAYER 7 : IN3
LAYER 8 : IN4(High)
LAYER 9 : SGND
LAYER 10 : BOT

BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	Power Diagram	1A

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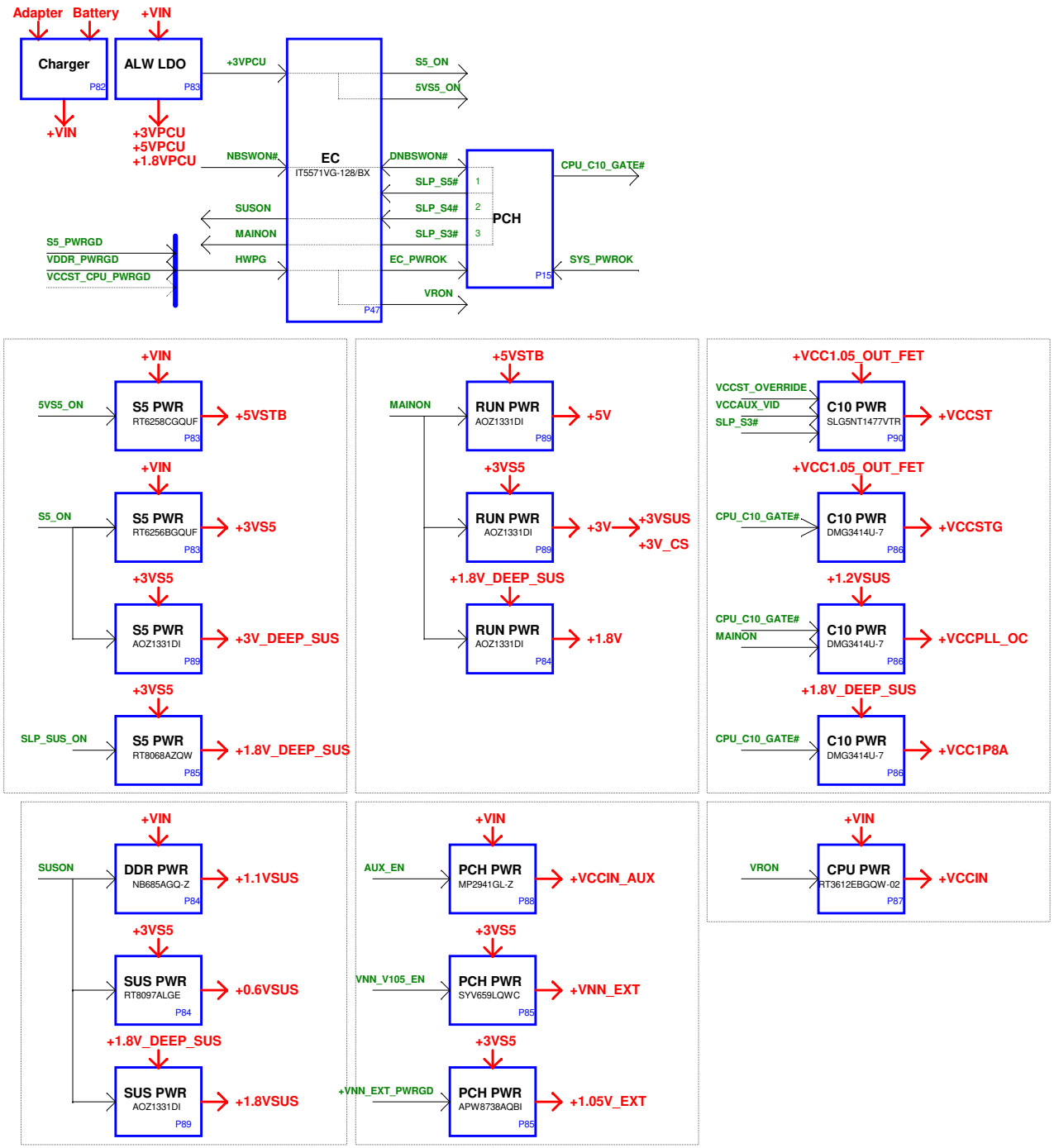
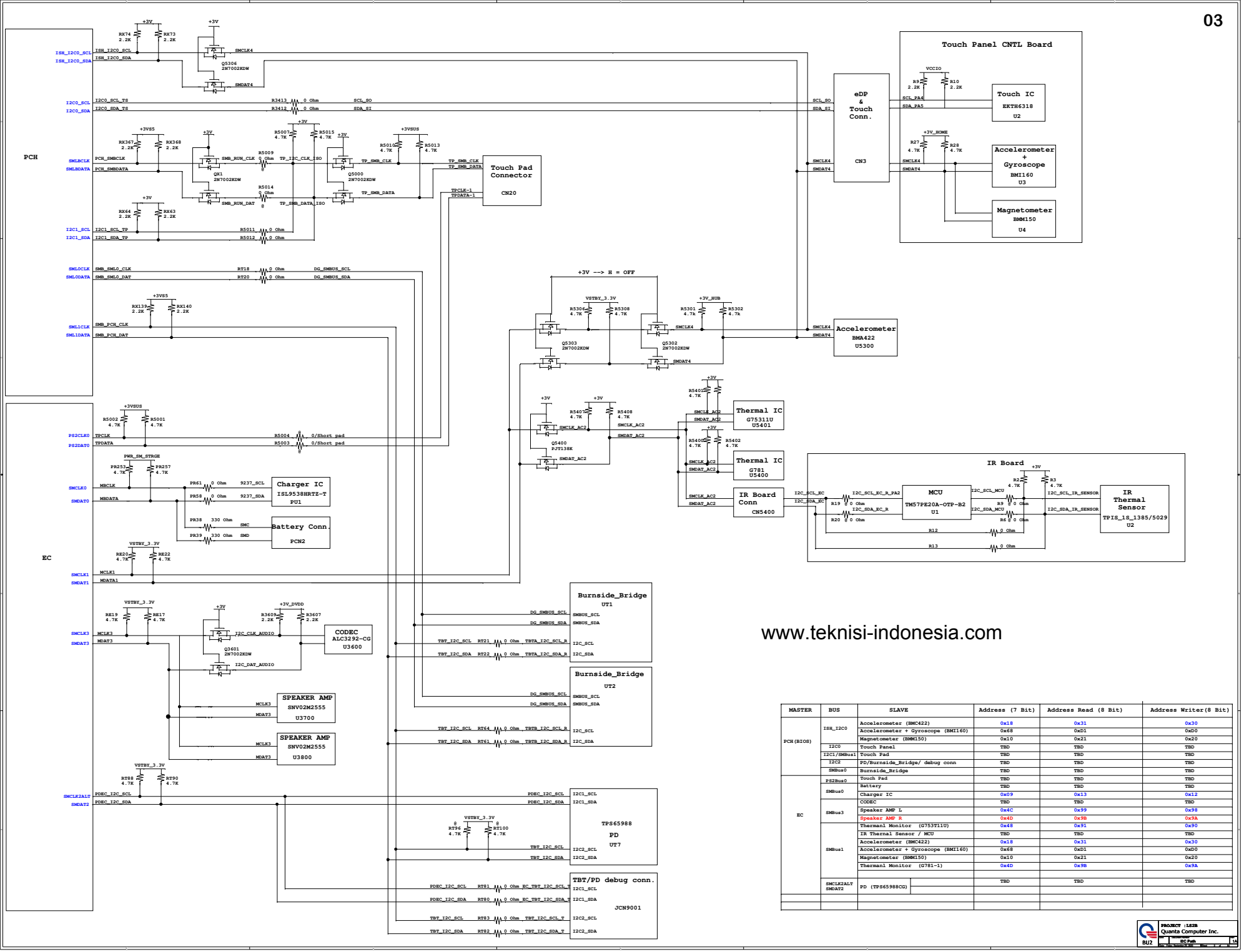


Main Power Rails

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+3V_WLAN_P	+3.3V	WLAN Power	CNVI_EN#	
+1.8VSUS	+1.8V	LPDDR4/4X Suspend Power	SUSON	
+0.6VSUS	+0.6V	LPDDR4/4X Suspend Power	SUSON	
+1.05V_EXT	+1.05V	PCH Power	+VNN_EXT_PWRGD	
+VNN_EXT	+1.05V	PCH Power	VNN_V105_EN	
+1.1VSUS	+1.1V	LPDDR4/4X Suspend Power	SUSON	
+1.8V	+1.8V	Audio Codec power	MAINON	
+1.8V_DEEP_SUS	+1.8V	PCH power	SLP_SUS_ON	
+3V	+3.3V	3V Run Power	MAINON	
+3VSUS	+3.3V	3V Suspend Power	MAINON	
+3VS5	+3.3V	3V S5 Power	S5_ON	
+3VPCU	+3.3V	3V Always Power	+VIN	
+5V	+5V	5V Run Power	MAINON	
+5VSTB	+5V	5V S5 Power	5VS5_ON	
+5VPCU	+5V	5V Always Power	+VIN	
+VCCIN_AUX	+1.8V	PCH Power	AUX_EN	
+VCCIN	SVID +1.89V(MAX)	CPU Core Power	VRON	
+VIN	+19V	AC power input		



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MASTER	BUS	SLAVE	Address (7 Bit)	Address Read (8 Bit)	Address Writer(8 Bit)
PCH(BIOS)	ISH_I2C0	Accelerometer (SMC422)	0x18	0x31	0x30
		Accelerometer + Gyroscope (BMI160)	0x68	0xD1	0xD0
		Magnetometer (BMM150)	0x10	0x21	0x20
	I2C0	Touch Panel	TBD	TBD	TBD
	I2C1/SMBus1	Touch Pad	TBD	TBD	TBD
	I2C2	PD/Burnside_Bridge/ debug conn	TBD	TBD	TBD
	SMBus0	Burnside_Bridge	TBD	TBD	TBD
EC	PS2Bus0	Touch Pad	TBD	TBD	TBD
	SMBus0	Battery	TBD	TBD	TBD
		Charger IC	0x09	0x13	0x12
	SMBus3	CODEC	TBD	TBD	TBD
		Speaker AMP L	0x4C	0x99	0x98
		Speaker AMP R	0x4D	0x9B	0x9A
	SMBus1	Thermal Monitor (G753711U)	0x48	0x91	0x90
		IR Thermal Sensor / MCU	TBD	TBD	TBD
		Accelerometer (SMC422)	0x18	0x31	0x30
		Accelerometer + Gyroscope (BMI160)	0x68	0xD1	0xD0
		Magnetometer (BMM150)	0x10	0x21	0x20
		Thermal Monitor (G781-1)	0x4D	0x9B	0x9A
	SMCLK2ALT SMDAT2		TBD	TBD	TBD
		PD (TPS65988CG)			

(008,011,012,13,15,016,17,56,061,80) +3V_DEEP_SUS

U7022A

eDP

(34)	INT_eDP_TXP3	INT_eDP_TXP3	AC2	DDIA_TXP_3
(34)	INT_eDP_TXN3	INT_eDP_TXN3	AC1	DDIA_TXN_3
(34)	INT_eDP_TXP2	INT_eDP_TXP2	AD2	DDIA_TXP_2
(34)	INT_eDP_TXN2	INT_eDP_TXN2	AD1	DDIA_TXN_2
(34)	INT_eDP_TXP1	INT_eDP_TXP1	AF1	DDIA_TXP_1
(34)	INT_eDP_TXN1	INT_eDP_TXN1	AF2	DDIA_TXN_1
(34)	INT_eDP_TXP0	INT_eDP_TXP0	AG2	DDIA_TXP_0
(34)	INT_eDP_TXN0	INT_eDP_TXN0	AG1	DDIA_TXN_0
(34)	INT_eDP_AUXP	INT_eDP_AUXP	AJ2	DDIA_AUX_P
(34)	INT_eDP_AUXN	INT_eDP_AUXN	AJ1	DDIA_AUX
			DN4	GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
			DT6	GPP_E23/DDPA_CTRLDATA
(34)	EDP_HPD	EDP_HPD	DR5	GPP_E14/DDSP_HPDA/DISP_MISCA

HDMI

(35)	IN_CLK	IN_CLK	T12	DDIB_TXP_3
(35)	IN_CLK#	IN_CLK#	T11	DDIB_TXN_3
(35)	IN_D0	IN_D0	Y11	DDIB_TXP_2
(35)	IN_D0#	IN_D0#	Y9	DDIB_TXN_2
(35)	IN_D1	IN_D1	T9	DDIB_TXP_1
(35)	IN_D1#	IN_D1#	P9	DDIB_TXN_1
(35)	IN_D2	IN_D2	V11	DDIB_TXP_0
(35)	IN_D2#	IN_D2#	V9	DDIB_TXN_0
			AB8	DDIB_AUX_P
			AD8	DDIB_AUX
(35)	DDPB_CLK	DDPB_CLK	DM29	GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
(35)	DDPB_DATA	DDPB_DATA	DK27	GPP_H17/DDPB_CTRLDATA
(35)	HDMI_HPD_CON	HDMI_HPD_CON	DG43	GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD
(17)	BOARD_ID8	BOARD_ID8	DG47	GPP_A21/DDPC_CTRLCLK/I2S5_TXD
(17)	BOARD_ID9	BOARD_ID9	DJ47	GPP_A22/DDPC_CTRLDATA/I2S5_RXD
(058)	TBT_LSX0_TXD	TBT_LSX0_TXD	DU8	GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
(012,058)	TBT_LSX0_RXD	TBT_LSX0_RXD	DV8	GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD
(059)	TBT_LSX1_TXD	TBT_LSX1_TXD	DF6	GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
(012,059)	TBT_LSX1_RXD	TBT_LSX1_RXD	DD6	GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD
			DN23	GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
(012)	TBT_LSX2_RXD	TBT_LSX2_RXD	DM23	GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK
(34)	LCD_BK_OFF	LCD_BK_OFF	DK23	GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
(012)	TBT_LSX3_RXD	TBT_LSX3_RXD	DN21	GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI
			DF43	GPP_A17/DISP_MISCC/I2S4_TXD
(061)	TBTA_HPD	R7073 *0_5%_2	DDSP_HPD1	DF45	GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK
(061)	TBTB_HPD	R78101 *0_5%_2	DDSP_HPD2	DF47	GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM
				DH52	GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
			USB_OC2#	DK45	GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK
(34)	PCH_DISP_ON	PCH_DISP_ON	DM8	EDP_VDDEN
(006,34)	PCH_LVDS_BLON	PCH_LVDS_BLON	DN8	EDP_BKLTEN
(34)	PCH_DPST_PWM	PCH_DPST_PWM	DG10	EDP_BKLTCTL

TGL_U_IP_EXT/BGA

TBTA

TCP0_TXRX_P1	AY2	TCP0_TXRX_P1	TCP0_TXRX_P1	(058)
TCP0_TXRX_N1	AY1	TCP0_TXRX_N1	TCP0_TXRX_N1	(058)
TCP0_TXRX_P0	BB1	TCP0_TXRX_P0	TCP0_TXRX_P0	(058)
TCP0_TXRX_N0	BB2	TCP0_TXRX_N0	TCP0_TXRX_N0	(058)
TCP0_TX_P1	AM5	TCP0_TX_P1	TCP0_TX_P1	(058)
TCP0_TX_N1	AM7	TCP0_TX_N1	TCP0_TX_N1	(058)
TCP0_TX_P0	AT7	TCP0_TX_P0	TCP0_TX_P0	(058)
TCP0_TX_N0	AT5	TCP0_TX_N0	TCP0_TX_N0	(058)
TCP0_AUX_P	AP7	TCP0_AUX_DP	TCP0_AUX_DP	(058)
TCP0_AUX	AP5	TCP0_AUX_DN	TCP0_AUX_DN	(058)

TBTB

TCP1_TXRX_P1	AT2	TCP1_TXRX_P1	TCP1_TXRX_P1	(059)
TCP1_TXRX_N1	AT1	TCP1_TXRX_N1	TCP1_TXRX_N1	(059)
TCP1_TXRX_P0	AU1	TCP1_TXRX_P0	TCP1_TXRX_P0	(059)
TCP1_TXRX_N0	AU2	TCP1_TXRX_N0	TCP1_TXRX_N0	(059)
TCP1_TX_P1	AD5	TCP1_TX_P1	TCP1_TX_P1	(059)
TCP1_TX_N1	AD7	TCP1_TX_N1	TCP1_TX_N1	(059)
TCP1_TX_P0	AH7	TCP1_TX_P0	TCP1_TX_P0	(059)
TCP1_TX_N0	AH5	TCP1_TX_N0	TCP1_TX_N0	(059)
TCP1_AUX_P	AF7	TCP1_AUX_DP	TCP1_AUX_DP	(059)
TCP1_AUX	AF5	TCP1_AUX_DN	TCP1_AUX_DN	(059)

TCP2_TXRX_P1	BF1	
TCP2_TXRX_N1	BF2	
TCP2_TXRX_P0	BE2	
TCP2_TXRX_N0	BE1	
TCP2_TX_P1	BD7	
TCP2_TX_N1	BD5	
TCP2_TX_P0	AY5	
TCP2_TX_N0	AY7	
TCP2_AUX_P	BB5	
TCP2_AUX	BB7	
TCP3_TXRX_P1	BK1	
TCP3_TXRX_N1	BK2	
TCP3_TXRX_P0	BJ2	
TCP3_TXRX_N0	BJ1	
TCP3_TX_P1	BM7	
TCP3_TX_N1	BM5	
TCP3_TX_P0	BH5	
TCP3_TX_N0	BH7	
TCP3_AUX_P	BK5	
TCP3_AUX	BK7	
TC_RCOMP_P	AN2	TCRCOMP_DP
TC_RCOMP	AN1	TCRCOMP_DN — R7360 150_1%_2
DSI_DE_TE_2	M8	DSI_DE_TE_2
DDI_RCOMP	AB1	DP_RCOMP
DISP_UTILS/DSI_DE_TE_1	CE4	DISP_UTILS — TP7019; R7369 150_1%_2; R7190 100K_1%_2

+3V_DEEP_SUS

R7066 10K_5%_2 USB_OC2#

R7061 100K_5%_2 EDP_HPD

need Check HPD Function

BU2	PROJECT : LS2B Quanta Computer Inc.	
Size Custom	Document Number TGL-U 1/14 (DDI/TBT/eDP)	Rev 1A
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Tiger Lake Processor DDR4

05

DDR CHANNEL A

DDR4 Non-IL

U7022B

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

(28)	M_A_DQ7	CP53	M_A_DQ7	DDR0_DQ0_7/DDR0_DQ0_7	DDR0_DQ0_7/DDR0_DQ0_7
(28)	M_A_DQ6	CP52	M_A_DQ6	DDR0_DQ0_6/DDR0_DQ0_6	DDR0_DQ0_6/DDR0_DQ0_6
(28)	M_A_DQ5	CP50	M_A_DQ5	DDR0_DQ0_5/DDR0_DQ0_5	DDR0_DQ0_5/DDR0_DQ0_5
(28)	M_A_DQ4	CP49	M_A_DQ4	DDR0_DQ0_4/DDR0_DQ0_4	DDR0_DQ0_4/DDR0_DQ0_4
(28)	M_A_DQ3	CU53	M_A_DQ3	DDR0_DQ0_3/DDR0_DQ0_3	DDR0_DQ0_3/DDR0_DQ0_3
(28)	M_A_DQ2	CU52	M_A_DQ2	DDR0_DQ0_2/DDR0_DQ0_2	DDR0_DQ0_2/DDR0_DQ0_2
(28)	M_A_DQ1	CU50	M_A_DQ1	DDR0_DQ0_1/DDR0_DQ0_1	DDR0_DQ0_1/DDR0_DQ0_1
(28)	M_A_DQ0	CU49	M_A_DQ0	DDR0_DQ0_0/DDR0_DQ0_0	DDR0_DQ0_0/DDR0_DQ0_0
(28)	M_A_DQ15	CH53	M_A_DQ15	DDR0_DQ1_7/DDR0_DQ1_7	DDR0_DQ1_7/DDR0_DQ1_7
(28)	M_A_DQ14	CH52	M_A_DQ14	DDR0_DQ1_6/DDR0_DQ1_6	DDR0_DQ1_6/DDR0_DQ1_6
(28)	M_A_DQ13	CH50	M_A_DQ13	DDR0_DQ1_5/DDR0_DQ1_5	DDR0_DQ1_5/DDR0_DQ1_5
(28)	M_A_DQ12	CH49	M_A_DQ12	DDR0_DQ1_4/DDR0_DQ1_4	DDR0_DQ1_4/DDR0_DQ1_4
(28)	M_A_DQ11	CL53	M_A_DQ11	DDR0_DQ1_3/DDR0_DQ1_3	DDR0_DQ1_3/DDR0_DQ1_3
(28)	M_A_DQ10	CL52	M_A_DQ10	DDR0_DQ1_2/DDR0_DQ1_2	DDR0_DQ1_2/DDR0_DQ1_2
(28)	M_A_DQ9	CL50	M_A_DQ9	DDR0_DQ1_1/DDR0_DQ1_1	DDR0_DQ1_1/DDR0_DQ1_1
(28)	M_A_DQ8	CL49	M_A_DQ8	DDR0_DQ1_0/DDR0_DQ1_0	DDR0_DQ1_0/DDR0_DQ1_0
(28)	M_A_DQ23	CT47	M_A_DQ23	DDR1_DQ2_7/DDR0_DQ2_7	DDR1_DQ2_7/DDR0_DQ2_7
(28)	M_A_DQ22	CV47	M_A_DQ22	DDR1_DQ2_6/DDR0_DQ2_6	DDR1_DQ2_6/DDR0_DQ2_6
(28)	M_A_DQ21	CT45	M_A_DQ21	DDR1_DQ2_5/DDR0_DQ2_5	DDR1_DQ2_5/DDR0_DQ2_5
(28)	M_A_DQ20	CV45	M_A_DQ20	DDR1_DQ2_4/DDR0_DQ2_4	DDR1_DQ2_4/DDR0_DQ2_4
(28)	M_A_DQ19	CT42	M_A_DQ19	DDR1_DQ2_3/DDR0_DQ2_3	DDR1_DQ2_3/DDR0_DQ2_3
(28)	M_A_DQ18	CV42	M_A_DQ18	DDR1_DQ2_2/DDR0_DQ2_2	DDR1_DQ2_2/DDR0_DQ2_2
(28)	M_A_DQ17	CT41	M_A_DQ17	DDR1_DQ2_1/DDR0_DQ2_1	DDR1_DQ2_1/DDR0_DQ2_1
(28)	M_A_DQ16	CV41	M_A_DQ16	DDR1_DQ2_0/DDR0_DQ2_0	DDR1_DQ2_0/DDR0_DQ2_0
(28)	M_A_DQ31	CK47	M_A_DQ31	DDR1_DQ3_7/DDR0_DQ3_7	DDR1_DQ3_7/DDR0_DQ3_7
(28)	M_A_DQ30	CM47	M_A_DQ30	DDR1_DQ3_6/DDR0_DQ3_6	DDR1_DQ3_6/DDR0_DQ3_6
(28)	M_A_DQ29	CK45	M_A_DQ29	DDR1_DQ3_5/DDR0_DQ3_5	DDR1_DQ3_5/DDR0_DQ3_5
(28)	M_A_DQ28	CM45	M_A_DQ28	DDR1_DQ3_4/DDR0_DQ3_4	DDR1_DQ3_4/DDR0_DQ3_4
(28)	M_A_DQ27	CK42	M_A_DQ27	DDR1_DQ3_3/DDR0_DQ3_3	DDR1_DQ3_3/DDR0_DQ3_3
(28)	M_A_DQ26	CM42	M_A_DQ26	DDR1_DQ3_2/DDR0_DQ3_2	DDR1_DQ3_2/DDR0_DQ3_2
(28)	M_A_DQ25	CM41	M_A_DQ25	DDR1_DQ3_1/DDR0_DQ3_1	DDR1_DQ3_1/DDR0_DQ3_1
(28)	M_A_DQ24	CK41	M_A_DQ24	DDR1_DQ3_0/DDR0_DQ3_0	DDR1_DQ3_0/DDR0_DQ3_0
(28)	M_A_DQ39	BF53	M_A_DQ39	DDR2_DQ0_7/DDR0_DQ4_7	DDR2_DQ0_7/DDR0_DQ4_7
(28)	M_A_DQ38	BF52	M_A_DQ38	DDR2_DQ0_6/DDR0_DQ4_6	DDR2_DQ0_6/DDR0_DQ4_6
(28)	M_A_DQ37	BF50	M_A_DQ37	DDR2_DQ0_5/DDR0_DQ4_5	DDR2_DQ0_5/DDR0_DQ4_5
(28)	M_A_DQ36	BF49	M_A_DQ36	DDR2_DQ0_4/DDR0_DQ4_4	DDR2_DQ0_4/DDR0_DQ4_4
(28)	M_A_DQ35	BH53	M_A_DQ35	DDR2_DQ0_3/DDR0_DQ4_3	DDR2_DQ0_3/DDR0_DQ4_3
(28)	M_A_DQ34	BH52	M_A_DQ34	DDR2_DQ0_2/DDR0_DQ4_2	DDR2_DQ0_2/DDR0_DQ4_2
(28)	M_A_DQ33	BH50	M_A_DQ33	DDR2_DQ0_1/DDR0_DQ4_1	DDR2_DQ0_1/DDR0_DQ4_1
(28)	M_A_DQ32	BH49	M_A_DQ32	DDR2_DQ0_0/DDR0_DQ4_0	DDR2_DQ0_0/DDR0_DQ4_0
(28)	M_A_DQ47	AY53	M_A_DQ47	DDR2_DQ1_7/DDR0_DQ5_7	DDR2_DQ1_7/DDR0_DQ5_7
(28)	M_A_DQ46	AY52	M_A_DQ46	DDR2_DQ1_6/DDR0_DQ5_6	DDR2_DQ1_6/DDR0_DQ5_6
(28)	M_A_DQ45	AY50	M_A_DQ45	DDR2_DQ1_5/DDR0_DQ5_5	DDR2_DQ1_5/DDR0_DQ5_5
(28)	M_A_DQ44	AY49	M_A_DQ44	DDR2_DQ1_4/DDR0_DQ5_4	DDR2_DQ1_4/DDR0_DQ5_4
(28)	M_A_DQ43	BC53	M_A_DQ43	DDR2_DQ1_3/DDR0_DQ5_3	DDR2_DQ1_3/DDR0_DQ5_3
(28)	M_A_DQ42	BC52	M_A_DQ42	DDR2_DQ1_2/DDR0_DQ5_2	DDR2_DQ1_2/DDR0_DQ5_2
(28)	M_A_DQ41	BC50	M_A_DQ41	DDR2_DQ1_1/DDR0_DQ5_1	DDR2_DQ1_1/DDR0_DQ5_1
(28)	M_A_DQ40	BC49	M_A_DQ40	DDR2_DQ1_0/DDR0_DQ5_0	DDR2_DQ1_0/DDR0_DQ5_0
(28)	M_A_DQ55	BK47	M_A_DQ55	DDR3_DQ0_7/DDR0_DQ6_7	DDR3_DQ0_7/DDR0_DQ6_7
(28)	M_A_DQ54	BK45	M_A_DQ54	DDR3_DQ0_6/DDR0_DQ6_6	DDR3_DQ0_6/DDR0_DQ6_6
(28)	M_A_DQ53	BH47	M_A_DQ53	DDR3_DQ0_5/DDR0_DQ6_5	DDR3_DQ0_5/DDR0_DQ6_5
(28)	M_A_DQ52	BH45	M_A_DQ52	DDR3_DQ0_4/DDR0_DQ6_4	DDR3_DQ0_4/DDR0_DQ6_4
(28)	M_A_DQ51	BH42	M_A_DQ51	DDR3_DQ0_3/DDR0_DQ6_3	DDR3_DQ0_3/DDR0_DQ6_3
(28)	M_A_DQ50	BK41	M_A_DQ50	DDR3_DQ0_2/DDR0_DQ6_2	DDR3_DQ0_2/DDR0_DQ6_2
(28)	M_A_DQ49	BH41	M_A_DQ49	DDR3_DQ0_1/DDR0_DQ6_1	DDR3_DQ0_1/DDR0_DQ6_1
(28)	M_A_DQ48	BD47	M_A_DQ48	DDR3_DQ0_0/DDR0_DQ6_0	DDR3_DQ0_0/DDR0_DQ6_0
(28)	M_A_DQ63	BD47	M_A_DQ63	DDR3_DQ1_7/DDR0_DQ7_7	DDR3_DQ1_7/DDR0_DQ7_7
(28)	M_A_DQ62	BB47	M_A_DQ62	DDR3_DQ1_6/DDR0_DQ7_6	DDR3_DQ1_6/DDR0_DQ7_6
(28)	M_A_DQ61	BD45	M_A_DQ61	DDR3_DQ1_5/DDR0_DQ7_5	DDR3_DQ1_5/DDR0_DQ7_5
(28)	M_A_DQ60	BB45	M_A_DQ60	DDR3_DQ1_4/DDR0_DQ7_4	DDR3_DQ1_4/DDR0_DQ7_4
(28)	M_A_DQ59	BB42	M_A_DQ59	DDR3_DQ1_3/DDR0_DQ7_3	DDR3_DQ1_3/DDR0_DQ7_3
(28)	M_A_DQ58	BB41	M_A_DQ58	DDR3_DQ1_2/DDR0_DQ7_2	DDR3_DQ1_2/DDR0_DQ7_2
(28)	M_A_DQ57	BD42	M_A_DQ57	DDR3_DQ1_1/DDR0_DQ7_1	DDR3_DQ1_1/DDR0_DQ7_1
(28)	M_A_DQ56	BD41	M_A_DQ56	DDR3_DQ1_0/DDR0_DQ7_0	DDR3_DQ1_0/DDR0_DQ7_0

DDR4/LP4/LP5/LP5 CMD Flip

BT42	DDR0_CLK_P1/DDR3_CLK_P/DDR3_CLK_P/DDR3_CLK_P			
BT41	DDR0_CLK_N1/DDR3_CLK_N/DDR3_CLK_N/DDR3_CLK			
BP52	NC/DDR2_CLK_P/DDR2_CLK_P/DDR2_CLK_P			
BP53	NC/DDR2_CLK_N/DDR2_CLK_N/DDR2_CLK			
CD42	NC/DDR1_CLK_P/DDR1_CLK_P/DDR1_CLK_P			
CD41	NC/DDR1_CLK_N/DDR1_CLK_N/DDR1_CLK			
CC52	DDR0_CLK_P0/DDR0_CLK_P/DDR0_CLK_P/DDR0_CLK_P	M_A_CLKP0	(28)	
CC53	DDR0_CLK_N0/DDR0_CLK_N/DDR0_CLK_N/DDR0_CLK	M_A_CLKN0	(28)	

DDR4/LP4/LP5/LP5 CMD Flip

BT45	NC/DDR3_CKE0/DDR3_WCK_P/DDR3_WCK_P			
BT47	NC/DDR3_CKE1/DDR3_WCK_N/DDR3_WCK			
BN51	NC/DDR2_CKE0/DDR2_WCK_P/DDR2_WCK_P			
BN53	NC/DDR2_CKE1/DDR2_WCK_N/DDR2_WCK			
CD45	NC/DDR1_CKE0/DDR1_WCK_P/DDR1_WCK_P			
CD47	NC/DDR1_CKE1/DDR1_WCK_N/DDR1_WCK			
CA51	NC/DDR0_CKE0/DDR0_WCK_P/DDR0_WCK_P			
CA53	NC/DDR0_CKE1/DDR0_WCK_N/DDR0_WCK			

DDR4/LP4/LP5/LP5 CMD Flip

BU52	DDR0_CKE1/DDR2_CA4/DDR2_CA5/DDR2_CA1			
BL50	DDR0_CKE0/DDR2_CA5/DDR2_CA6/DDR2_CA0	M_A_CKE0	(28)	

DDR4/LP4/LP5/LP5 CMD Flip

CF42	DDR0_CS1/DDR1_CA1/DDR1_CA1/DDR1_CA5			
CF47	DDR0_CS0/NC/DDR1_CS1/DDR1_CA4	M_A_CS#0	(28)	

DDR4/LP4/LP5/LP5 CMD Flip

CE53	NC/DDR0_CA0/DDR0_CA0/DDR0_CA6			
CE50	NC/DDR0_CA1/DDR0_CA1/DDR0_CA5			
BL53	NC/DDR2_CS0/DDR2_CA2/DDR2_CA2			
BP47	NC/DDR3_CA5/DDR3_CA6/DDR3_CA0			
BP42	NC/DDR3_CA4/DDR3_CA5/DDR3_CA1			
BP45	NC/DDR3_CA3/DDR3_CA4/DDR3_CS1			
BP44	NC/DDR3_CA2/DDR3_CA3/DDR3_CS0			

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

BB44	M_A_DQSP7	DDR3_DQSP_1/DDR0_DQSP_7/DDR1_DQSP_3	M_A_DQSP7	(28)	(29)
BD44	M_A_DQSN7	DDR3_DQSN_1/DDR0_DQSN_7/DDR1_DQSN_3	M_A_DQSN7	(28)	(29)
BK44	M_A_DQSP6	DDR3_DQSP_0/DDR0_DQSP_6/DDR1_DQSP_2	M_A_DQSP6	(28)	(29)
BH44	M_A_DQSN6	DDR3_DQSN_0/DDR0_DQSN_6/DDR1_DQSN_2	M_A_DQSN6	(28)	(29)
BA51	M_A_DQSP5	DDR2_DQSP_1/DDR0_DQSP_5/DDR0_DQSP_3	M_A_DQSP5	(28)	(29)
BA50	M_A_DQSN5	DDR2_DQSN_1/DDR0_DQSN_5/DDR0_DQSN_3	M_A_DQSN5	(28)	(29)
BG51	M_A_DQSP4	DDR2_DQSP_0/DDR0_DQSP_4/DDR0_DQSP_2	M_A_DQSP4	(28)	(29)
BG50	M_A_DQSN4	DDR2_DQSN_0/DDR0_DQSN_4/DDR0_DQSN_2	M_A_DQSN4	(28)	(29)
CK44	M_A_DQSP3	DDR1_DQSP_1/DDR0_DQSP_3/DDR1_DQSP_1	M_A_DQSP3	(28)	(29)
CM44	M_A_DQSN3	DDR1_DQSN_1/DDR0_DQSN_3/DDR1_DQSN_1	M_A_DQSN3	(28)	(29)
CT44	M_A_DQSP2	DDR1_DQSP_0/DDR0_DQSP_2/DDR1_DQSP_0	M_A_DQSP2	(28)	(29)
CV44	M_A_DQSN2	DDR1_DQSN_0/DDR0_DQSN_2/DDR1_DQSN_0	M_A_DQSN2	(28)	(29)
CK51	M_A_DQSP1	DDR0_DQSP_1/DDR0_DQSP_1/DDR0_DQSP_1	M_A_DQSP1	(28)	(29)
CK50	M_A_DQSN1	DDR0_DQSN_1/DDR0_DQSN_1/DDR0_DQSN_1	M_A_DQSN1	(28)	(29)
CR51	M_A_DQSP0	DDR0_DQSP_0/DDR0_DQSP_0/DDR0_DQSP_0	M_A_DQSP0	(28)	(29)
CR50	M_A_DQSN0	DDR0_DQSN_0/DDR0_DQSN_0/DDR0_DQSN_0	M_A_DQSN0	(28)	(29)

DDR4/LP4/LP5/LP5 CMD Flip

CF44	DDR0_ODT1/DDR1_CA0/DDR1_CA0/DDR1_CA6			
CF45	DDR0_ODT0/DDR1_CS0/DDR1_CA2/DDR1_CA2	M_A_ODT0	(28)	

DDR4/LP4/LP5/LP5 CMD Flip

CB47	M_A_A16	DDR0_MA16/DDR1_CA4/DDR1_CA5/DDR1_CA1	M_A_A16	(28)
CB44	M_A_A15	DDR0_MA15/DDR1_CA3/DDR1_CA4/DDR1_CS1	M_A_A15	(28)
CB45	M_A_A14	DDR0_MA14/DDR1_CA2/DDR1_CA3/DDR1_CS0	M_A_A14	(28)
CF41	M_A_A13	DDR0_MA13/DDR1_CS1/DDR1_CS0/DDR1_CA3	M_A_A13	(28)
BU53	M_A_A12	DDR0_MA12/DDR2_CA1/DDR2_CA1/DDR2_CA5	M_A_A12	(28)
BT51	M_A_A11	DDR0_MA11/NC/DDR2_CS1/DDR2_CA4	M_A_A11	(28)
BV42	M_A_A10	DDR0_MA10/DDR3_CA1/DDR3_CA1/DDR3_CA5	M_A_A10	(28)
BU50	M_A_A9	DDR0_MA9/DDR2_CA0/DDR2_CA0/DDR2_CA6	M_A_A9	(28)
BY53	M_A_A8	DDR0_MA8/DDR0_CA2/DDR0_CA3/DDR0_CS0	M_A_A8	(28)
CA50	M_A_A7	DDR0_MA7/DDR0_CA4/DDR0_CA5/DDR0_CA1	M_A_A7	(28)
BY52	M_A_A6	DDR0_MA6/DDR0_CA3/DDR0_CA4/DDR0_CS1	M_A_A6	(28)
BY50	M_A_A5	DDR0_MA5/DDR0_CA5/DDR0_CA6/DDR0_CA0	M_A_A5	(28)
CD51	M_A_A4	DDR0_MA4/DDR0_CS0/DDR0_CA2/DDR0_CA2	M_A_A4	(28)
CD53	M_A_A3	DDR0_MA3/DDR0_CS1/DDR0_CS0/DDR0_CA3	M_A_A3	(28)
BV47	M_A_A2	DDR0_MA2/DDR3_CS0/DDR3_CS2/DDR3_CA2	M_A_A2	(28)
CE52	M_A_A1	DDR0_MA1/NC/DDR0_CS1/DDR0_CA4	M_A_A1	(28)
BV41	M_A_A0	DDR0_MA0/NC/DDR3_CS1/DDR3_CA4	M_A_A0	(28)

DDR4/LP4/LP5/LP5 CMD Flip

BN50	DDR0_BG1/DDR2_CA2/DDR2_CA3/DDR2_CS0	M_A_BG_1	(28)	
BL52	DDR0_BG0/DDR2_CA3/DDR2_CA4/DDR2_CS1	M_A_BG_0	(28)	

DDR4/LP4/LP5/LP5 CMD Flip

CB42	DDR0_BA1/DDR1_CA5/DDR1_CA6/DDR1_CA0	M_A_BA_1	(28)	
BV44	DDR0_BA0/DDR3_CA0/DDR3_CA0/DDR3_CA6	M_A_BA_0	(28)	

DDR4/LP4/LP5/LP5 CMD Flip

BT53	DDR0_ACT#/DDR2_CS1/DDR2_CS0/DDR2_CA3	DDRA_ACT#	(28)	

DDR4/LP4/LP5/LP5 CMD Flip

BV45	DDR0_PAR/DDR3_CS1/DDR3_CS0/DDR3_CA3	DDR0_PAR	(28)	

AU50	DDR0_ALERT#	DDR0_ALERT#	(28)	
AU49	DDR0_VREF_CA	SMDDR_VREF_DQ0_M3	(28)	

E52	DDR_VTT_CTRL			
DV47	DRAM_RESET#			
C49	DDR_RCOMP0	R7170 100 1% 2		

DDR_VTT_CTL

DRAM_RESET#

DDR_RCOMP

TGL_U_IP_EXT/BGA

DDR CHANNEL B

DDR4 Non-IL

U7022C

LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

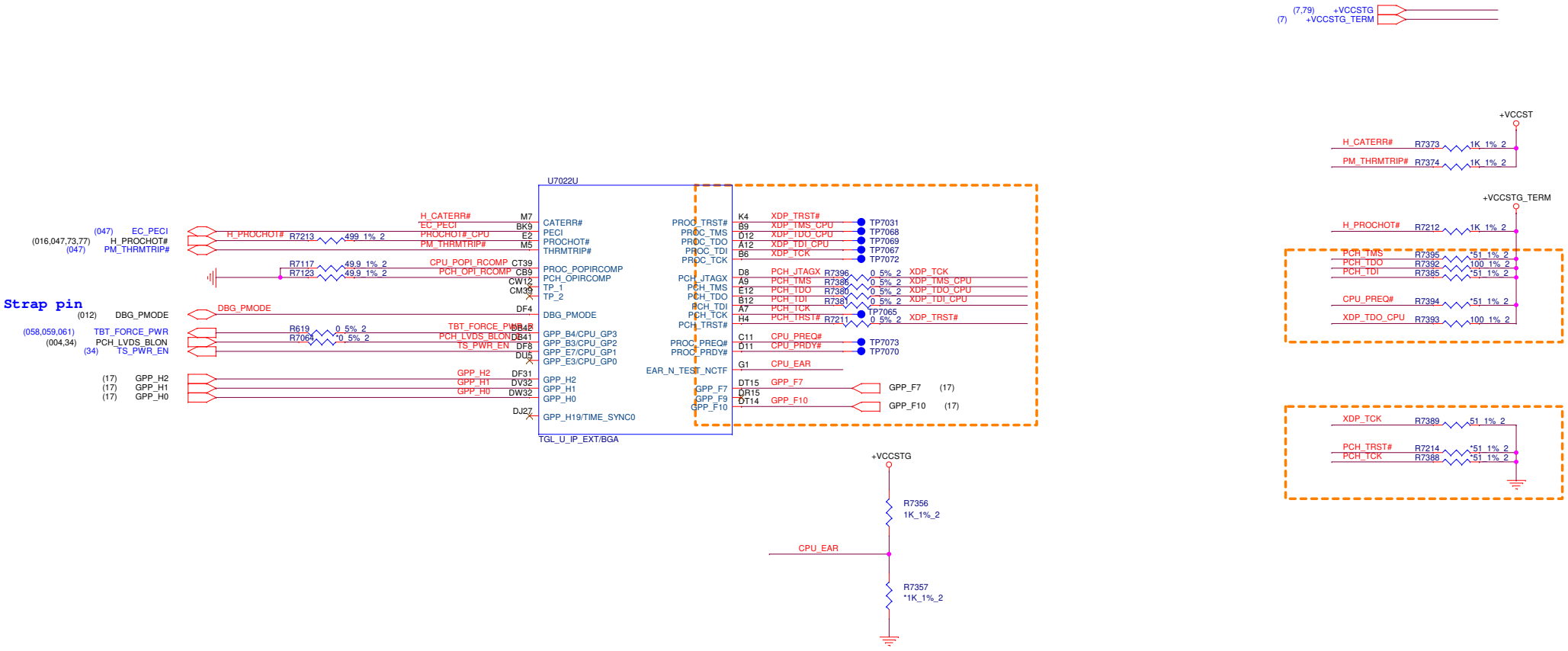
(29)	M_B_DQ7	AL53	M_B_DQ7	DDR4_DQ0_7/DDR1_DQ0_7	DDR4_DQ0_7/DDR0_DQ4_7
(29)	M_B_DQ6	AL52	M_B_DQ6	DDR4_DQ0_6/DDR1_DQ0_6	DDR4_DQ0_6/DDR0_DQ4_6
(29)	M_B_DQ5	AL50	M_B_DQ5	DDR4_DQ0_5/DDR1_DQ0_5	DDR4_DQ0_5/DDR0_DQ4_5
(29)	M_B_DQ4	AL49	M_B_DQ4	DDR4_DQ0_4/DDR1_DQ0_4	DDR4_DQ0_4/DDR0_DQ4_4
(29)	M_B_DQ3	AP53	M_B_DQ3	DDR4_DQ0_3/DDR1_DQ0_3	DDR4_DQ0_3/DDR0_DQ4_3
(29)	M_B_DQ2	AP52	M_B_DQ2	DDR4_DQ0_2/DDR1_DQ0_2	DDR4_DQ0_2/DDR0_DQ4_2
(29)	M_B_DQ1	AP50	M_B_DQ1	DDR4_DQ0_1/DDR1_DQ0_1	DDR4_DQ0_1/DDR0_DQ4_1
(29)	M_B_DQ0	AP49	M_B_DQ0	DDR4_DQ0_0/DDR1_DQ0_0	DDR4_DQ0_0/DDR0_DQ4_0
(29)	M_B_DQ15	AF53	M_B_DQ15	DDR4_DQ1_7/DDR1_DQ1_7	DDR4_DQ1_7/DDR0_DQ5_7
(29)	M_B_DQ14	AF52	M_B_DQ14	DDR4_DQ1_6/DDR1_DQ1_6	DDR4_DQ1_6/DDR0_DQ5_6
(29)	M_B_DQ13	AF50	M_B_DQ13	DDR4_DQ1_5/DDR1_DQ1_5	DDR4_DQ1_5/DDR0_DQ5_5
(29)	M_B_DQ12	AF49	M_B_DQ12	DDR4_DQ1_4/DDR1_DQ1_4	DDR4_DQ1_4/DDR0_DQ5_4
(29)	M_B_DQ11	AH53	M_B_DQ11	DDR4_DQ1_3/DDR1_DQ1_3	DDR4_DQ1_3/DDR0_DQ5_3
(29)	M_B_DQ10	AH52	M_B_DQ10	DDR4_DQ1_2/DDR1_DQ1_2	DDR4_DQ1_2/DDR0_DQ5_2
(29)	M_B_DQ9	AH50	M_B_DQ9	DDR4_DQ1_1/DDR1_DQ1_1	DDR4_DQ1_1/DDR0_DQ5_1
(29)	M_B_DQ8	AH49	M_B_DQ8	DDR4_DQ1_0/DDR1_DQ1_0	DDR4_DQ1_0/DDR0_DQ5_0
(29)	M_B_DQ23	AR41	M_B_DQ23	DDR5_DQ0_7/DDR1_DQ2_7	DDR5_DQ0_7/DDR0_DQ2_7
(29)	M_B_DQ22	AV42	M_B_DQ22	DDR5_DQ0_6/DDR1_DQ2_6	DDR5_DQ0_6/DDR0_DQ2_6
(29)	M_B_DQ21	AR42	M_B_DQ21	DDR5_DQ0_5/DDR1_DQ2_5	DDR5_DQ0_5/DDR0_DQ2_5
(29)	M_B_DQ20	AV41	M_B_DQ20	DDR5_DQ0_4/DDR1_DQ2_4	DDR5_DQ0_4/DDR0_DQ2_4
(29)	M_B_DQ19	AR45	M_B_DQ19	DDR5_DQ0_3/DDR1_DQ2_3	DDR5_DQ0_3/DDR0_DQ2_3
(29)	M_B_DQ18	AV45	M_B_DQ18	DDR5_DQ0_2/DDR1_DQ2_2	DDR5_DQ0_2/DDR0_DQ2_2
(29)	M_B_DQ17	AR47	M_B_DQ17	DDR5_DQ0_1/DDR1_DQ2_1	DDR5_DQ0_1/DDR0_DQ2_1
(29)	M_B_DQ16	AV47	M_B_DQ16	DDR5_DQ0_0/DDR1_DQ2_0	DDR5_DQ0_0/DDR0_DQ2_0
(29)	M_B_DQ31	AJ41	M_B_DQ31	DDR5_DQ1_7/DDR1_DQ3_7	DDR5_DQ1_7/DDR0_DQ3_7
(29)	M_B_DQ30	AJ42	M_B_DQ30	DDR5_DQ1_6/DDR1_DQ3_6	DDR5_DQ1_6/DDR0_DQ3_6
(29)	M_B_DQ29	AL41	M_B_DQ29	DDR5_DQ1_5/DDR1_DQ3_5	DDR5_DQ1_5/DDR0_DQ3_5
(29)	M_B_DQ28	AL42	M_B_DQ28	DDR5_DQ1_4/DDR1_DQ3_4	DDR5_DQ1_4/DDR0_DQ3_4
(29)	M_B_DQ27	AJ45	M_B_DQ27	DDR5_DQ1_3/DDR1_DQ3_3	DDR5_DQ1_3/DDR0_DQ3_3
(29)	M_B_DQ26	AJ47	M_B_DQ26	DDR5_DQ1_2/DDR1_DQ3_2	DDR5_DQ1_2/DDR0_DQ3_2
(29)	M_B_DQ25	AL45	M_B_DQ25	DDR5_DQ1_1/DDR1_DQ3_1	DDR5_DQ1_1/DDR0_DQ3_1
(29)	M_B_DQ24	AL47	M_B_DQ24	DDR5_DQ1_0/DDR1_DQ3_0	DDR5_DQ1_0/DDR0_DQ3_0
(29)	M_B_DQ39	A43	M_B_DQ39	DDR6_DQ0_7/DDR1_DQ4_7	DDR6_DQ0_7/DDR0_DQ6_7
(29)	M_B_DQ38	B43	M_B_DQ38	DDR6_DQ0_6/DDR1_DQ4_6	DDR6_DQ0_6/DDR0_DQ6_6
(29)	M_B_DQ37	D43	M_B_DQ37	DDR6_DQ0_5/DDR1_DQ4_5	DDR6_DQ0_5/DDR0_DQ6_5
(29)	M_B_DQ36	E44	M_B_DQ36	DDR6_DQ0_4/DDR1_DQ4_4	DDR6_DQ0_4/DDR0_DQ6_4
(29)	M_B_DQ35	A46	M_B_DQ35	DDR6_DQ0_3/DDR1_DQ4_3	DDR6_DQ0_3/DDR0_DQ6_3
(29)	M_B_DQ34	B46	M_B_DQ34	DDR6_DQ0_2/DDR1_DQ4_2	DDR6_DQ0_2/DDR0_DQ6_2
(29)	M_B_DQ33	D46	M_B_DQ33	DDR6_DQ0_1/DDR1_DQ4_1	DDR6_DQ0_1/DDR0_DQ6_1
(29)	M_B_DQ32	E47	M_B_DQ32	DDR6_DQ0_0/DDR1_DQ4_0	DDR6_DQ0_0/DDR0_DQ6_0
(29)	M_B_DQ47	E38	M_B_DQ47	DDR6_DQ1_7/DDR1_DQ5_7	DDR6_DQ1_7/DDR0_DQ7_7
(29)	M_B_DQ46	D38	M_B_DQ46	DDR6_DQ1_6/DDR1_DQ5_6	DDR6_DQ1_6/DDR0_DQ7_6
(29)	M_B_DQ45	B38	M_B_DQ45	DDR6_DQ1_5/DDR1_DQ5_5	DDR6_DQ1_5/DDR0_DQ7_5
(29)	M_B_DQ44	A38	M_B_DQ44	DDR6_DQ1_4/DDR1_DQ5_4	DDR6_DQ1_4/DDR0_DQ7_4
(29)	M_B_DQ43	E41	M_B_DQ43	DDR6_DQ1_3/DDR1_DQ5_3	DDR6_DQ1_3/DDR0_DQ7_3
(29)	M_B_DQ42	D40	M_B_DQ42	DDR6_DQ1_2/DDR1_DQ5_2	DDR6_DQ1_2/DDR0_DQ7_2
(29)	M_B_DQ41	B40	M_B_DQ41	DDR6_DQ1_1/DDR1_DQ5_1	DDR6_DQ1_1/DDR0_DQ7_1
(29)	M_B_DQ40	A40	M_B_DQ40	DDR6_DQ1_0/DDR1_DQ5_0	DDR6_DQ1_0/DDR0_DQ7_0
(29)	M_B_DQ55	G42	M_B_DQ55	DDR7_DQ0_7/DDR1_DQ6_7	DDR7_DQ0_7/DDR0_DQ6_7
(29)	M_B_DQ54	G41	M_B_DQ54	DDR7_DQ0_6/DDR1_DQ6_6	DDR7_DQ0_6/DDR0_DQ6_6
(29)	M_B_DQ53	J41	M_B_DQ53	DDR7_DQ0_5/DDR1_DQ6_5	DDR7_DQ0_5/DDR0_DQ6_5
(29)	M_B_DQ52	J42	M_B_DQ52	DDR7_DQ0_4/DDR1_DQ6_4	DDR7_DQ0_4/DDR0_DQ6_4
(29)	M_B_DQ51	G45	M_B_DQ51	DDR7_DQ0_3/DDR1_DQ6_3	DDR7_DQ0_3/DDR0_DQ6_3
(29)	M_B_DQ50	J45	M_B_DQ50	DDR7_DQ0_2/DDR1_DQ6_2	DDR7_DQ0_2/DDR0_DQ6_2
(29)	M_B_DQ49	G47	M_B_DQ49	DDR7_DQ0_1/DDR1_DQ6_1	DDR7_DQ0_1/DDR0_DQ6_1
(29)	M_B_DQ48	J47	M_B_DQ48	DDR7_DQ0_0/DDR1_DQ6_0	DDR7_DQ0_0/DDR0_DQ6_0
(29)	M_B_DQ63	G38	M_B_DQ63	DDR7_DQ1_7/DDR1_DQ7_7	DDR7_DQ1_7/DDR0_DQ7_7
(29)	M_B_DQ62	G36	M_B_DQ62	DDR7_DQ1_6/DDR1_DQ7_6	DDR7_DQ1_6/DDR0_DQ7_6
(29)	M_B_DQ61	H36	M_B_DQ61	DDR7_DQ1_5/DDR1_DQ7_5	DDR7_DQ1_5/DDR0_DQ7_5
(29)	M_B_DQ60	H38	M_B_DQ60	DDR7_DQ1_4/DDR1_DQ7_4	DDR7_DQ1_4/DDR0_DQ7_4
(29)	M_B_DQ59	N36	M_B_DQ59	DDR7_DQ1_3/DDR1_DQ7_3	DDR7_DQ1_3/DDR0_DQ7_3
(29)	M_B_DQ58	L36	M_B_DQ58	DDR7_DQ1_2/DDR1_DQ7_2	DDR7_DQ1_2/DDR0_DQ7_2
(29)	M_B_DQ57	L38	M_B_DQ57	DDR7_DQ1_1/DDR1_DQ7_1	DDR7_DQ1_1/DDR0_DQ7_1
(29)	M_B_DQ56	N38	M_B_DQ56	DDR7_DQ1_0/DDR1_DQ7_0	DDR7_DQ1_0/DDR0_DQ7_0

DDR4/LP4/LP5/LP5 CMD Flip

R41	DDR1_CLK_P1/DDR7_CLK_P/DDR7_CLK_P/DDR7_CLK_P			
R42	DDR1_CLK_N1/DDR7_CLK_N/DDR7_CLK_N/DDR7_CLK			
M52	NC/DDR6_CLK_P/DDR6_CLK_P/DDR6_CLK_P			
M53	NC/DDR6_CLK_N/DDR6_CLK_N/DDR6_CLK			
AC42	NC/DDR5_CLK_P/DDR5_CLK_P/DDR5_CLK_P			
AC41	NC/DDR5_CLK_N/DDR5_CLK_N/DDR5_CLK			
Y52	DDR1_CLK_P0/DDR4_CLK_P/DDR4_CLKP/DDR4_CLK_P	M_B_CLKP0	(29)	
Y53	DDR1_CLK_N0/DDR4_CLK_N/DDR4_CLK_N/DDR4_CLK	M_B_CLKN0	(29)	

DDR4/LP4/LP5/LP5 CMD Flip

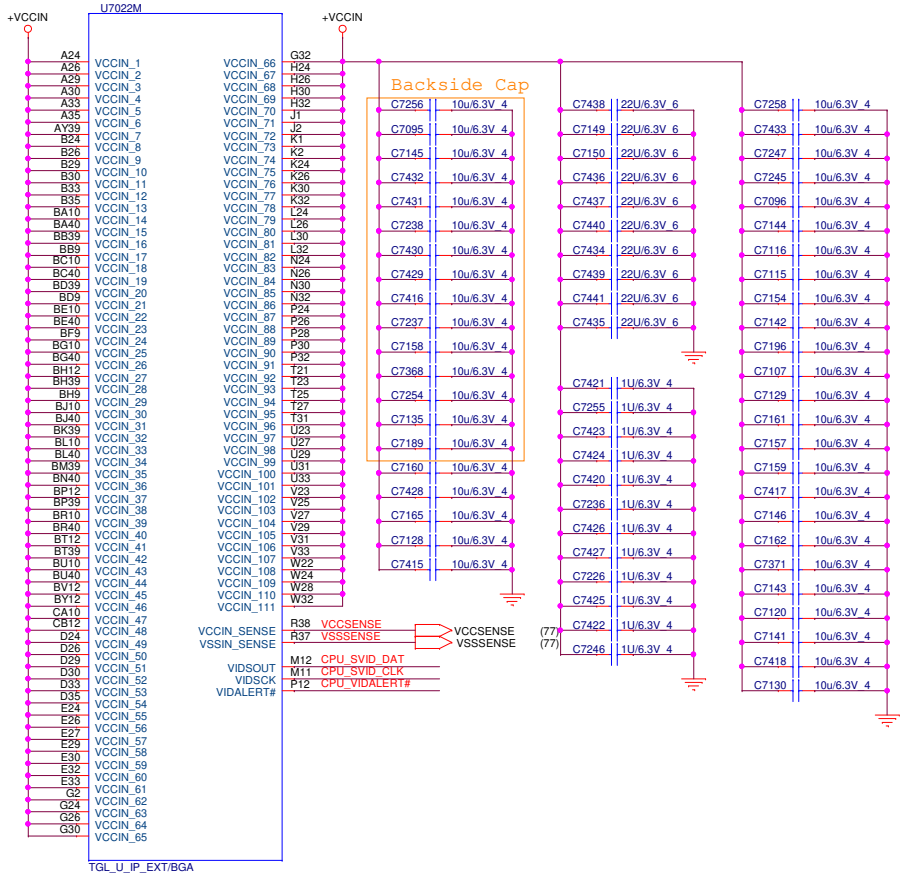
R47	NC/DDR7_CKE0/DDR7_WCK_P/DDR7_WCK_P			
R45	NC/DDR7_CKE1/DDR7_WCK_N/DDR7_WCK			
K51	NC/DDR6_CKE0/DDR6_WCK_P/DDR6_WCK_P			
K53	NC/DDR6_CKE1/DDR6_WCK_N/DDR6_WCK			
AC47	NC/DDR5_CKE0/DDR5_WCK_P/DDR5_WC



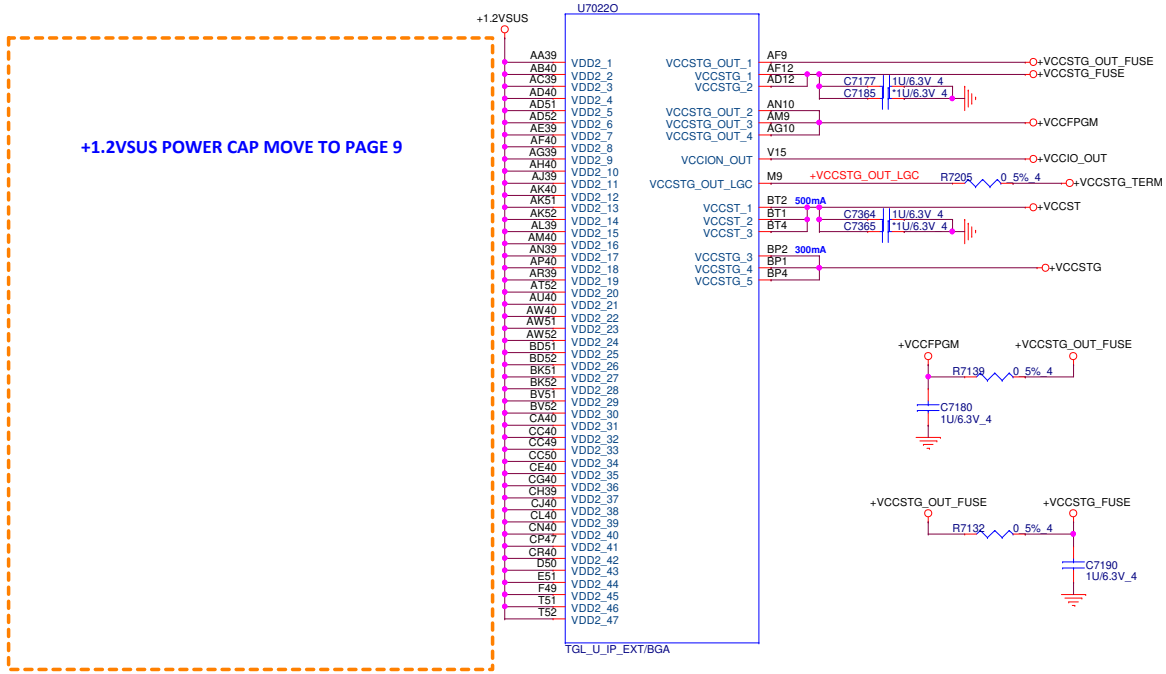
BU2	PROJECT : LS2B Quanta Computer Inc.	
Size Custom	Document Number TGL-U 3/14 (CPU MISC/JTA)	Rev 1A
Date: Friday, September 25, 2020	Sheet 006 of 105	

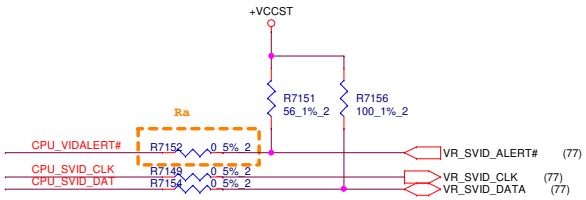
+VCCIN (23,77)
+VCCIO_OUT (10)
+VCCST (006,15,047,77,79)
+VCCSTG (006,79)

+VCCIN: 65A



+1.2VSUS: 1.5A





ALERT# needs to Place between CLK and DAT
Ra Neen check value

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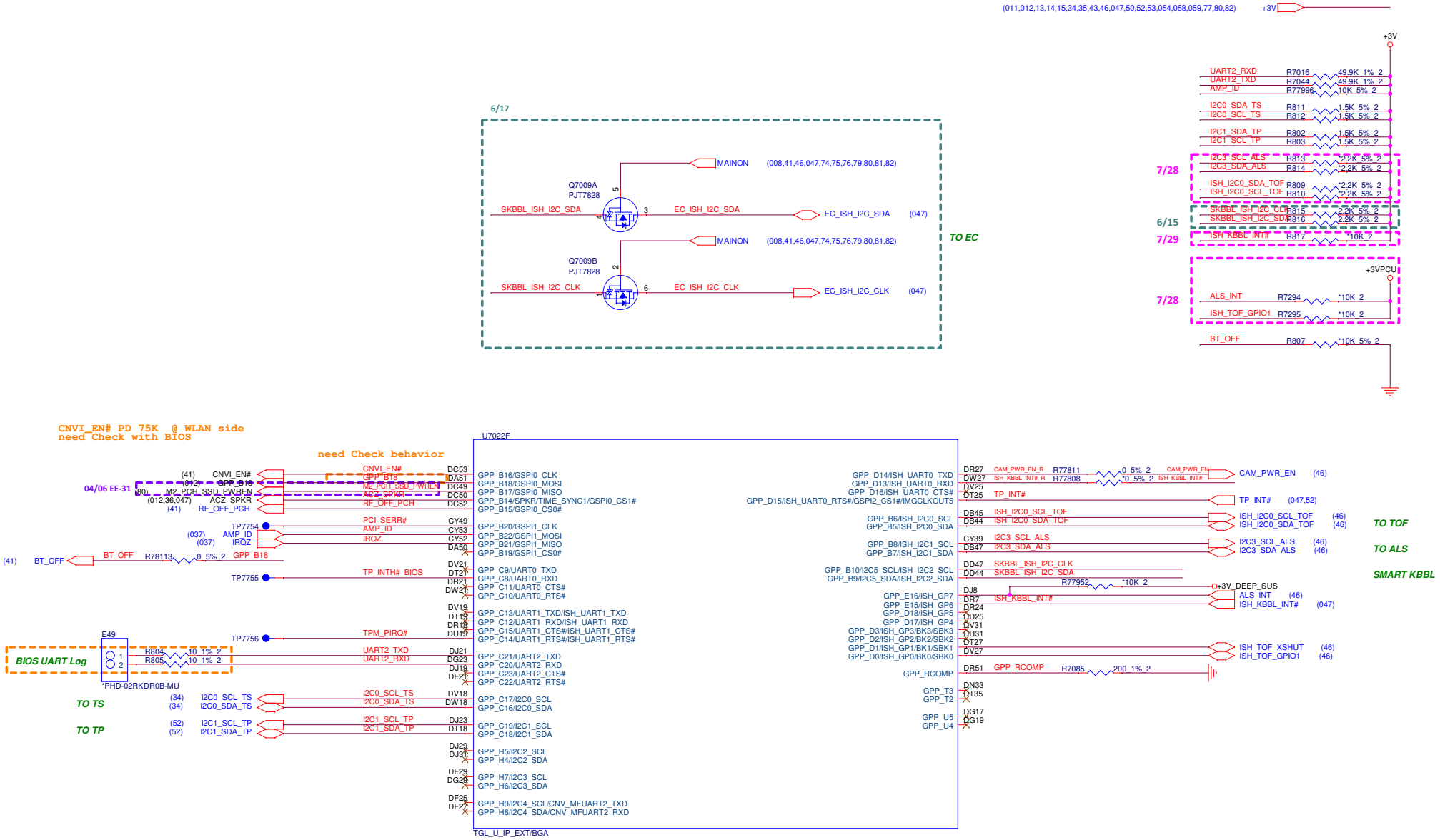
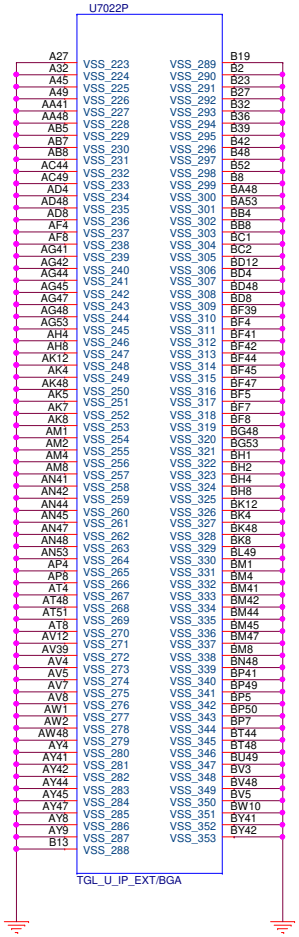
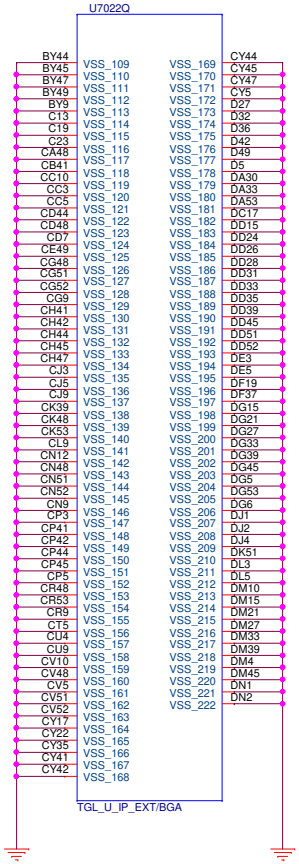
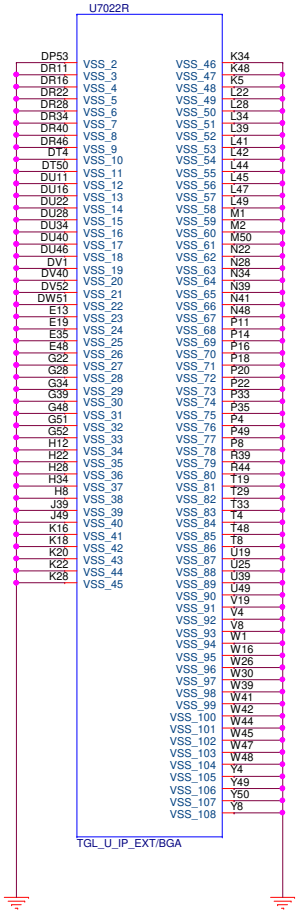
BU2	**PROJECT : LS2B** Quanta Computer Inc.	
Size Custom	Document Number TGL-U 4/14 (VCCIN/VDDQ)	Rev 1A
Date: Friday, September 25, 2020	Sheet 7 of 84	

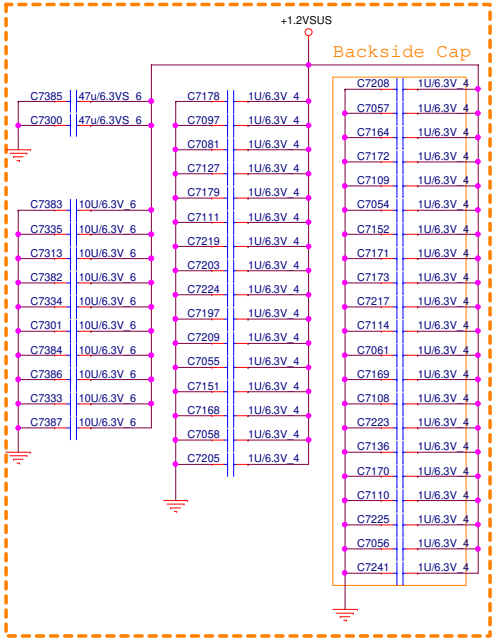


BU2	**PROJECT : LS2B**
	Quanta Computer Inc.
Size: Custom	Document Number: TGL-U 5/14 (I2C/ISH) — Rev: 1A
Date: Friday, September 25, 2020	Sheet 008 of 105

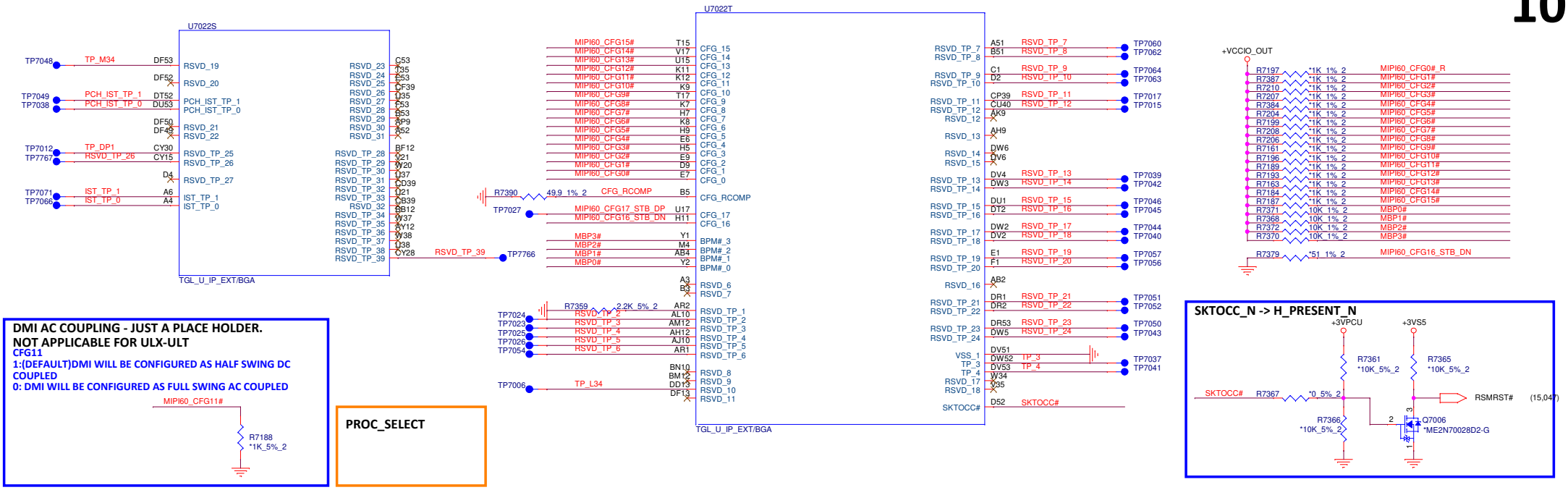








BU2	PROJECT : LS2B Quanta Computer Inc.		
	Size Custom	Document Number TGL-U 6/14 (GND)	Rev 1A
	Date: Friday, September 25, 2020	Sheet 9 of 84	



DMI AC COUPLING - JUST A PLACE HOLDER. NOT APPLICABLE FOR ULX-ULT

CFG11

1:(DEFAULT)DMI WILL BE CONFIGURED AS HALF SWING DC COUPLED

0: DMI WILL BE CONFIGURED AS FULL SWING AC COUPLED

MIPI60_CFG11# — R7188 *1K_5%_2

PROC_SELECT

SKTOCC_N -> H_PRESENT_N

PM SYNC LEGACY

CFG12

1: (DEFAULT) PMSYNC 2.0

0: LEGACY

MIPI60_CFG12# — R7192 *1K_5%_2

PMSYNC AYNC MODE- PM SYNC

CFG13

1: (DEFAULT)SYNCHCRONOUS (1 24 MHZ CYCLE PER BIT)

0: ASYNC - 4-24MHZ CYCLES PER BIT

MIPI60_CFG13# — R7169 *1K_5%_2

NO SVID PROTOCOL CAPABLE VR CONNECTED

CFG9

1: VRS SUPPORTING SVID PROTOCOL ARE PRESENT

0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

MIPI60_CFG9# — R7162 *1K_5%_2

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EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED

CFG0

1: (DEFAULT) NORMAL OPERATION; NO STALL

MIPI60_CFG0# — R7191 0_5%_2 — MIPI60_CFG0#_R — TP7029 — R7194 *1K_5%_2

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS

CFG2

1: (DEFAULT)NORMAL OPERATION

0: LANE REVERSAL

MIPI60_CFG2# — R7209 *1K_5%_2

PHYSICAL_DEBUG_ENABLED(DFX PRIVACY)

CFG4

1: DISABLED

AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT

0: ENABLED

NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

MIPI60_CFG4# — R7383 1K_5%_2

PEG DEFER TRAINING

CFG7

1: (DEFAULT) PEG TRAIN IMMEEDIATELY FOLLOWING XXRESETB DEASSERTION

0: PEG WAIT FOR BIOS FOR TRAINING

MIPI60_CFG7# — R7202 *1K_5%_2

SAFE MODE BOOT

CFG10

1: POWER FEATURES ACTIVATED DURING RESETT

0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

MIPI60_CFG10# — R7195 *1K_5%_2

PCH/ PCH LESS MODE SELECTION

CFG1

1: (DEFAULT) NORMAL OPERATION

0: PCH-LESS MODE

MIPI60_CFG1# — R7382 *1K_5%_2

PHYSICAL_DEBUG_ENABLED(DFX PRIVACY)

CFG3

1: DISABLED

0: ENABLED

SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

MIPI60_CFG3# — R7201 *1K_5%_2

PCIE PORT BIFURCATION STRAPS

CFG[6:5]

11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED

10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED

01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED

00 DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

MIPI60_CFG5# — R7203 *1K_5%_2

MIPI60_CFG6# — R7198 *1K_5%_2

ALLOW THE USE OF NOA ON LOCKED UNITS

CFG8

1: DISABLED(DEFAULT): IN THHIS CASE, NOA WILL BE DISABLE IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS

0: ENABLED: NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

MIPI60_CFG8# — R7200 *1K_5%_2

MIPI60_CFG14# — R7185 *1K_5%_2

MIPI60_CFG15# — R7168 *1K_5%_2

BU2

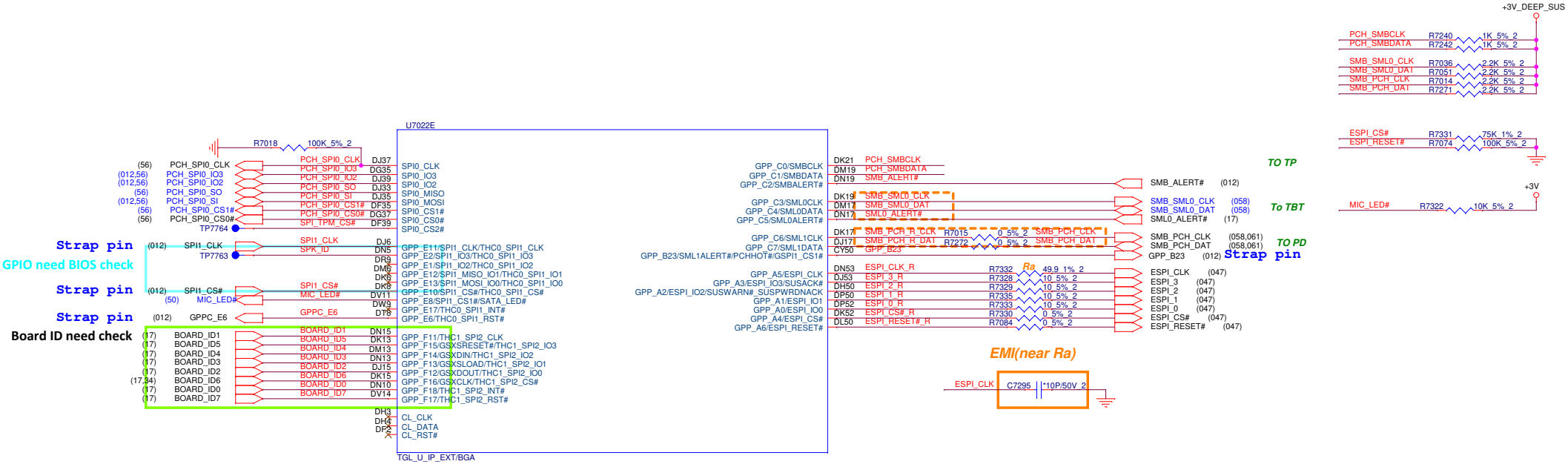
PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	TGL-U 7/14 (RSVD/XDP)	1A

Date: Friday, September 25, 2020 | Sheet 10 of 84

(004,008,012,13,15,016,17,56,061,80) +3V_DEEP_SUS
(008,012,13,14,15,34,35,43,46,047,50,52,53,054,058,059,77,80,82) +3V



PROJECT : LS2B	
Quanta Computer Inc.	
Size: Custom	Document Number: TGL-U 8/14 (SMBus/SPI)
Rev: 1A	
Date: Friday, September 25, 2020	Sheet 011 of 105

BU2

(004,058) TBT_LSX0_RXD — TBT_LSX0_RXD
(004,059) TBT_LSX1_RXD — TBT_LSX1_RXD
(004) TBT_LSX2_RXD — TBT_LSX2_RXD
(004) TBT_LSX3_RXD — TBT_LSX3_RXD

(004,008,011,13,15,016,17,56,061,80) +3V_DEEP_SUS
(008,011,13,14,15,34,35,43,46,047,50,52,53,054,058,059,77,80,82) +3V
(5,10,15,016,41,047,52,53,058,059,74,75,76,78,79,80) +3VS5
(14,016,41,047,76,80) +1.8V_DEEP_SUS
(016,79) +VCC1.05_OUT_FET
(14,016,73) +BAT_RTC

TOP SWAP OVERRIDE

High: TOP SWAP ENABLED
Low: DISABLED
WEAK INTERNAL PD 20K

GPP_B14/SPKR

(008,36,047) ACZ_SPKR — ACZ_SPKR — +3V — R7325 *4.7K_5%_2 — R7326 *20K_1%_2

TBT LSX PINS VCCIO CONFIGURATION

3V_S5 +3V_DEEP_SUS

GPP_E19 — R7300 *4.7K_5%_2 — TBT_LSX0_RXD — R7301 *20K_1%_2
GPP_E21 — R7042 *4.7K_5%_2 — TBT_LSX1_RXD — R7041 *20K_1%_2
GPP_D10 — R7291 *4.7K_5%_2 — TBT_LSX2_RXD — R7316 *20K_1%_2
GPP_D12 — R7292 *4.7K_5%_2 — TBT_LSX3_RXD — R7317 *20K_1%_2

WEAK INT. PD 20K

High: 3.3V
Low: 1.8V
NO INTERNAL PU/PD

(RSVD) BOOT HALT

High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_MOSI

3V_S5 +3V_DEEP_SUS — R7000 100K_1%_2
(011,56) PCH_SPI0_SI — PCH_SPI0_SI — R7006 1K_5%_2 — XDP_PCH_SPI0_SI — TP7000
R7004 *4.7K_5%_2

NO REBOOT

High: NO REBOOT
Low: REBOOT ENABLED
WEAK INTERNAL PD 20K

04/06 EE-28

GPP_B18/GSPI0_MOSI

+3V — R7060 4.7K_5%_2
(008) GPP_B18 — GPP_B18 — R7068 *20K_1%_2

01/15 PD 10K at PAGE.8

(RSVD) A0 PERSONALITY STRAP

High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_IO3

3V_S5 +3V_DEEP_SUS — R7005 100K_5%_2
(011,56) PCH_SPI0_IO3 — PCH_SPI0_IO3 — R7010 *4.7K_5%_2

M.2 CNVi Mode Select

High: Integrated CNVi disabled
Low: Integrated CNVi enabled
An external pull-up or pull-down is required

GPP_F2

+1.8V_DEEP_SUS — R7244 100K_5%_2
(14) CNV_RGI_DT_R — CNV_RGI_DT_R — R7256 *4.7K_5%_2

(RSVD) CONSENT STRAP

High: DISABLE
Low: ENABLE
External pull-up is required.

SPI0_IO2

3V_S5 +3V_DEEP_SUS — R7011 20K_1%_2
(011,56) PCH_SPI0_IO2 — PCH_SPI0_IO2 — R7013 1K_5%_2 — XDP_PCH_SPI0_IO2 — TP7002
R7012 *4.7K_5%_2

CPUNSSC CLOCK FREQ

High: 19.2MHz CLOCK FROM INTERNAL DIVIDER
Low: 38.4MHz CLOCK FROM DIRECT CRYSTAL (Default)
WEAK INTERNAL PD 20K

GPP_B23/SML1ALERT#

3V_S5 +3V_DEEP_SUS — R7323 *4.7K_5%_2
(011) GPP_B23 — GPP_B23 — R7324 *20K_1%_2

TLS CONFIDENTIALITY

GPP_C2/SMBALERT#

3V_S5 +3V_DEEP_SUS — +1.8V_DEEP_SUS
R7270 *4.7K_5%_2 — R7261 4.7K_5%_2
(011) SMB_ALERT# — SMB_ALERT# — R7269 *20K_1%_2

HIGH - TLS CONFIDENTIALITY ENABLE
LOW - TLS CONFIDENTIALITY DISABLE
WEAK INTERNAL PD 20K

(RSVD) JTAG ODT DISABLE

High: JTAG ODT Enable
Low: JTAG ODT Disable
External pull-up is required.

GPP_E6

3V_S5 +3V_DEEP_SUS — +1.8V_DEEP_SUS
R7299 *100K_5%_2 — R7298 100K_5%_2
(011) GPPC_E6 — GPPC_E6 — R7278 *4.7K_5%_2

Flash Descriptor Security Override

High: DISABLE
Low: ENABLE
WEAK INTERNAL PD 20K

GPP_R2

3V_S5 +3V_DEEP_SUS — R7286 *4.7K_5%_2
(15) ACZ_SDOUT — ACZ_SDOUT
(047) GPIO33_EC — R7285 1K_5%_2

THC0_SPI1_CLK

HVM ONLY

THC0_SPI1 Clock: THC SPI1 clock output from PCH. Supports 20 MHz, 33 MHz and 50 MHz.

+1.8V_DEEP_SUS — 3V_S5 +3V_DEEP_SUS — R7020 20K_1%_2 — R7021 *20K_1%_2
(011) SPI1_CLK
GPP_E11 — R7022 *20K_1%_2

MAF/SAF STRAP

High: SAF ENABLE
Low: MAF ENABLE
WEAK INTERNAL PD 20K

GPP_H3

3V_S5 +3V_DEEP_SUS — R7024 *2.2K_5%_2
(15) WIFI_WAKE# — WIFI_WAKE# — R7046 *20K_1%_2

(RSVD) ITP PMODE

High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K

+VCC1.05_OUT_FET — R7105 1K_5%_2
(006) DBG_PMODE — TP7011 — R7106 *20K_1%_2

ITP_PMODE

Reduce leakage from Coin Cell Batt

High: ENABLE
Low: DISABLE

INTRUDER#

+BAT_RTC — R7258 1M_5%_2
(15) INTRUDER# — INTRUDER# — R7282 *1M_5%_2

THC0_SPI1_CS#

HVM ONLY

THC0_SPI1 Chip Select: Used to select the touch devices if it is connected to THC0_SPI1 interface.

+1.8V_DEEP_SUS — 3V_S5 +3V_DEEP_SUS — R7037 20K_1%_2 — R7048 *20K_1%_2
(011) SPI1_CS#
GPP_E10 — R7047 *20K_1%_2

(RSVD) XTAL INPUT MODE

High: XTAL INPUT IS SINGLE ENDED
Low: XTAL IS ATTACHED
WEAK INTERNAL PD 20K

GPD7

+3VS5 — R7249 *4.7K_5%_2
(15) PCH_TBT_PERST# — PCH_TBT_PERST# — R7248 *20K_1%_2

XTAL FREQUENCE SEL

High: 24MHZ
(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
Low: 38.4MHZ (DEFAULT)
WEAK INTERNAL PD 20K

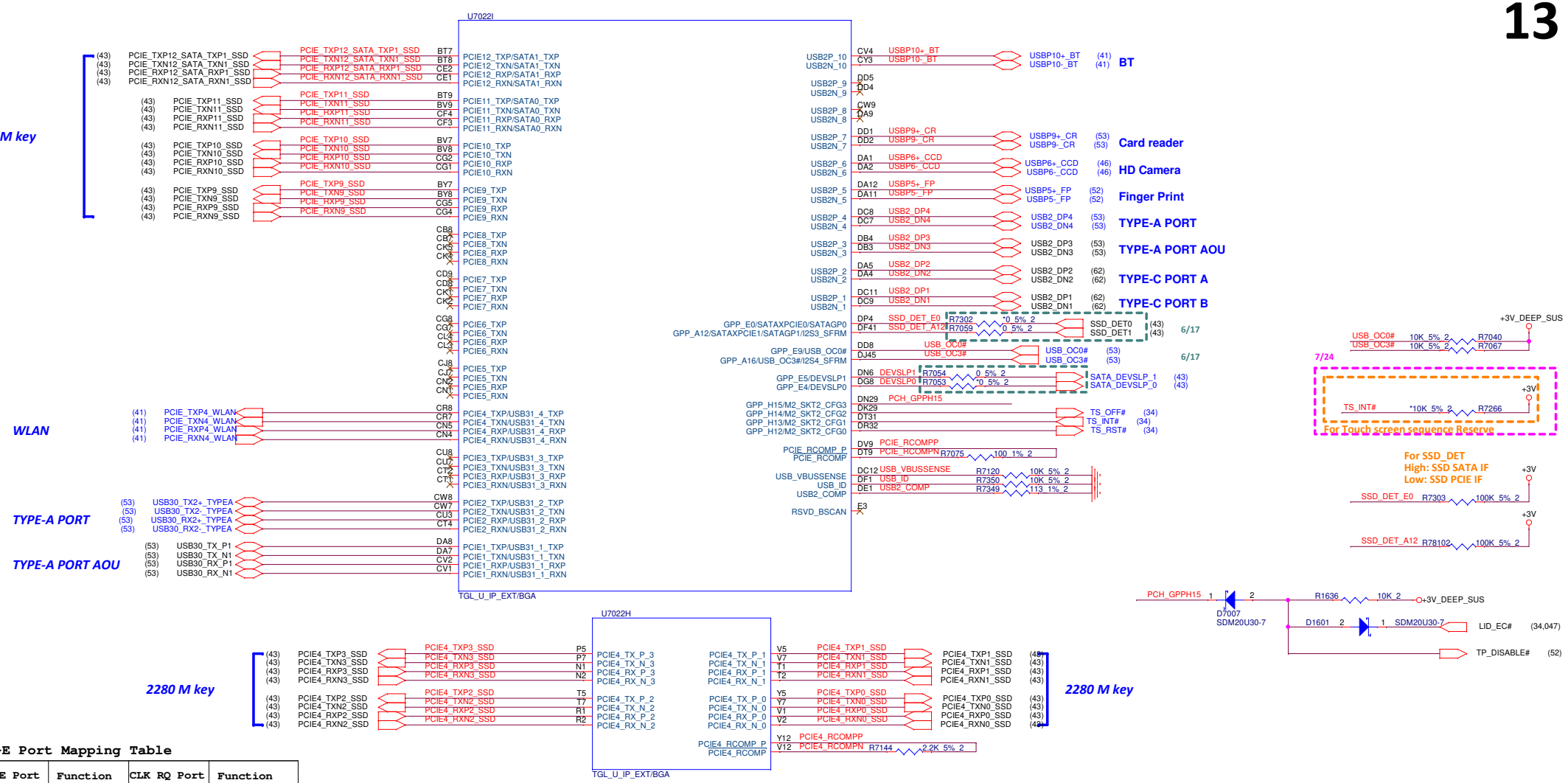
+1.8V_DEEP_SUS — R7008 *4.7K_5%_2
(14) CNV_BRI_DT_R — CNV_BRI_DT_R
GPP_F0 — R7017 *20K_1%_2

3V SELECT STRAP

0 = SPI voltage is 3.3V (4.7K ohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K ohm pull-up to DSW_PWROK)

3V_S5 +3V_DEEP_SUS — R7310 *4.7K_5%_2
(15) INPUT3VSEL — INPUT3VSEL — R7311 4.7K_5%_2

Because page size limited, some strap pin move to page 17



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PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	SSD-2280
Port2	Un-used	Port1	Un-used
Port3	Un-used	Port2	SSD-2242
Port4	WLAN	Port3	WLAN
Port5	Un-used	Port4	Un-used
Port6	Un-used	Port5	Un-used
Port7	Un-used	Port6	Un-used
Port8	Un-used		
Port9	SSD-2242		
Port10	SSD-2242		
Port11	SSD-2242		
Port12	SSD/SATA1 2242		

PCI-E 4.0 Port Mapping Table

USB3.0	Function
PORT-1	SSD-2280
PORT-2	SSD-2280
PORT-3	SSD-2280
PORT-4	SSD-2280

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0(SB) AOU
PORT-2	USB3.0(SB)
PORT-3	NC
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	TYPE-C PORT B
PORT-2	TYPE-C PORT A
PORT-3	USB3.0(SB) AOU
PORT-4	USB3.0(SB)
PORT-5	Finger Print
PORT-6	Camera
PORT-7	Card reader
PORT-8	NC
PORT-9	NC
PORT-10	CNVI BT

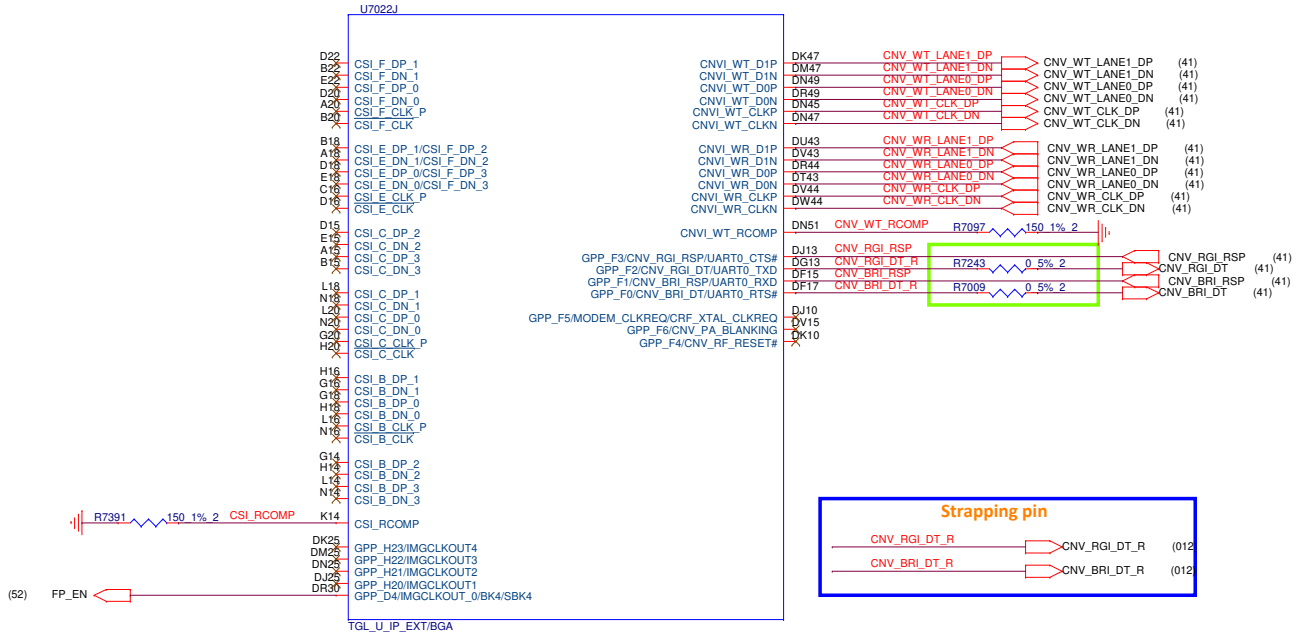
BU2

PROJECT :LS2B

Quanta Computer Inc.

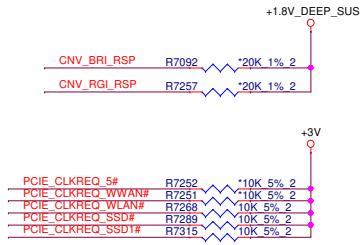
Size	Document Number	Rev
Custom	TGL-U 10/14(USB/PCIE/SAT)	1A

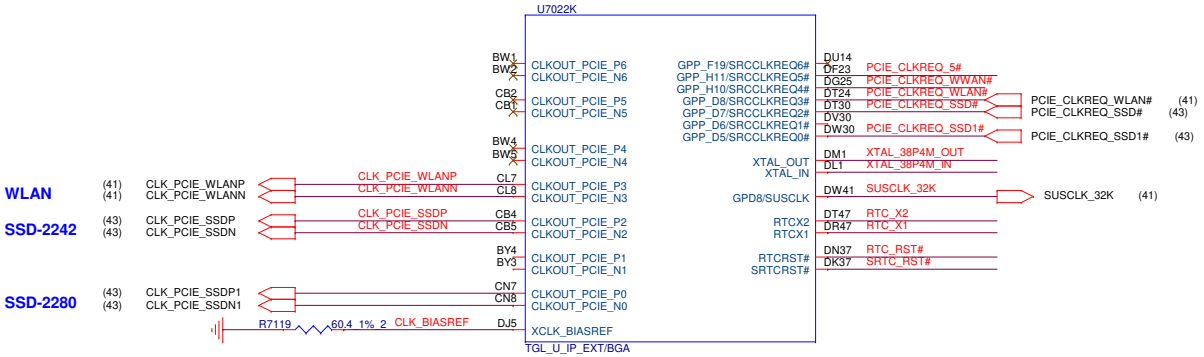
Date: Friday, September 25, 2020 Sheet 13 of 84



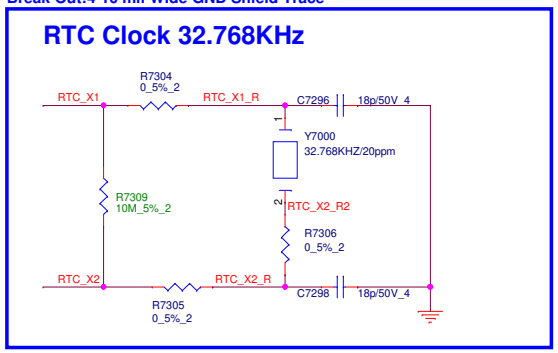
Strapping pin

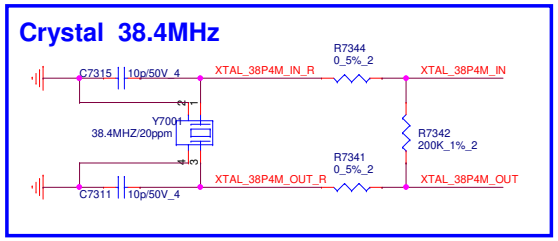
CNV_RGI_DT_R — CNV_RGI_DT_R (012
CNV_BRI_DT_R — CNV_BRI_DT_R (012

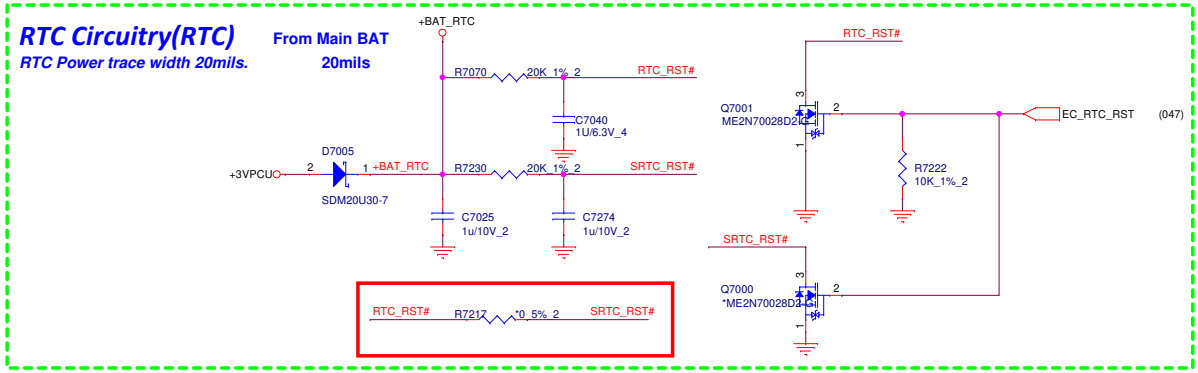




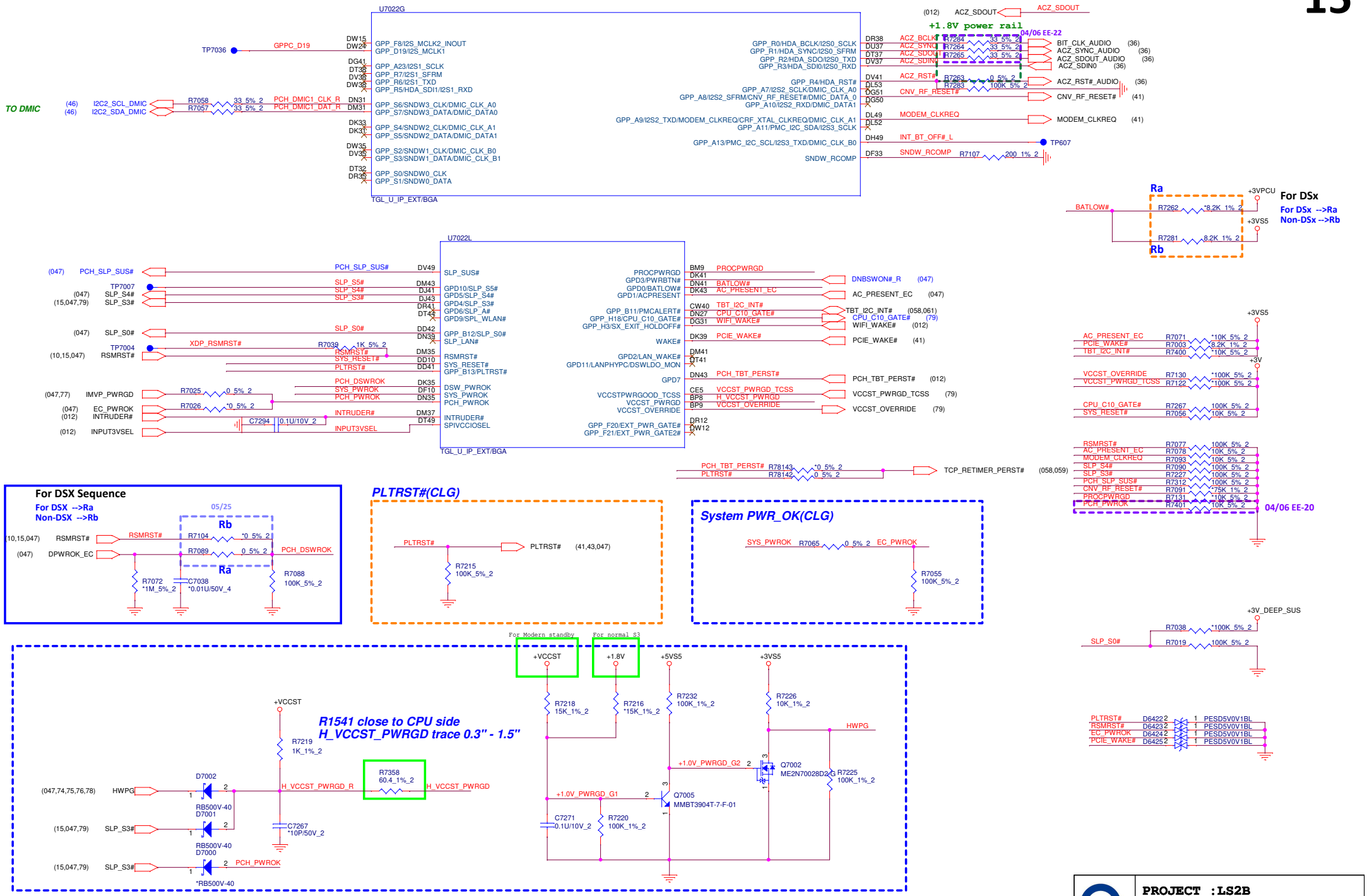
Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace







BU2	**PROJECT : LS2B** Quanta Computer Inc.
Size Custom	Document Number TGL-U 11/14(CSI/CNVI/CLK) — Rev 1A
Date: Friday, September 25, 2020	Sheet 14 of 84



BU2	**PROJECT : LS2B**
	Quanta Computer Inc.
Size: Custom	Document Number: TGL-U 12/14(PM/HDA/SD3.0) — Rev: 1A
Date: Friday, September 25, 2020	Sheet 15 of 105

+VCCIN_AUX (23,78)
+BAT_RTC (012,14,73)
+VNN_EXT (76)
+1.05V_EXT (76)
+1.8V_DEEP_SUS (012,14,41,047,76,80)
+3VS5 (5,10,012,15,41,047,52,53,058,059,74,75,76,78,79,80)

+VCCIN_AUX: 27A

+VCCIN_AUX

U7022N

C7342 47u/6.3VS_6
C7072 47u/6.3VS_6
C7126 47u/6.3VS_6
C7330 47u/6.3VS_6

C7121 22U/6.3V_6
C7337 22U/6.3V_6
C7331 22U/6.3V_6
C7341 22U/6.3V_6
C7166 22U/6.3V_6
C7125 22U/6.3V_6
C7133 22U/6.3V_6
C7340 22U/6.3V_6
C7123 22U/6.3V_6
C7167 22U/6.3V_6
C7122 22U/6.3V_6
C7124 22U/6.3V_6

C7339 10U/10V_4
C7092 10U/10V_4
C7332 10U/10V_4
C7326 10U/10V_4
C7325 10U/10V_4
C7079 10U/10V_4
C7078 10U/10V_4
C7088 10U/10V_4
C7077 10U/10V_4
C7329 10U/10V_4
C7328 10U/10V_4
C7083 10U/10V_4
C7104 10U/10V_4
C7195 10U/10V_4
C7084 10U/10V_4

Backside Cap
C7181 10U/10V_4
C7199 10U/10V_4
C7085 10U/10V_4
C7106 10U/10V_4
C7148 10U/10V_4
C7206 10U/10V_4
C7176 10U/10V_4
C7113 10U/10V_4
C7153 10U/10V_4
C7327 10U/10V_4

AB12 VCCIN_AUX_1
AC10 VCCIN_AUX_2
AE10 VCCIN_AUX_3
AK2 VCCIN_AUX_4
AR10 VCCIN_AUX_5
AT12 VCCIN_AUX_6
AU10 VCCIN_AUX_7
AW10 VCCIN_AUX_8
BV1 VCCIN_AUX_9
BV39 VCCIN_AUX_10
BW40 VCCIN_AUX_11
BY39 VCCIN_AUX_12
CC1 VCCIN_AUX_13
CD12 VCCIN_AUX_14
CF10 VCCIN_AUX_15
CG12 VCCIN_AUX_16
CH10 VCCIN_AUX_17
CJ1 VCCIN_AUX_18
CJ12 VCCIN_AUX_19
CK10 VCCIN_AUX_20
CL12 VCCIN_AUX_21
CM10 VCCIN_AUX_22
CP1 VCCIN_AUX_23
CP10 VCCIN_AUX_24
CR12 VCCIN_AUX_25
CT10 VCCIN_AUX_26
CU12 VCCIN_AUX_27
CY1 VCCIN_AUX_28
AK1 VCCIN_AUX_29

for Volume option

(78) VSS_AUX_SENSE — VSS_AUX_SENSE — AV9 VCCIN_AUX_VSSSENSE
(78) VCC_AUX_SENSE — VCC_AUX_SENSE — AT9 VCCIN_AUX_VCCSENSE

03/31 EE-15
R7121 100K_1%_2 +VNN_EXT — 500mA DD17 VCC_VNNEXT_1P05_1; DD18 VCC_VNNEXT_1P05_2
R7118 100K_1%_2 +1.05V_EXT — 500mA DA15 VCC_V1P05EXT_1P05_1; DA17 VCC_V1P05EXT_1P05_2

VRALERT# — DB39 GPP_B2/VRALERT#
TP7074 — DV12 GPP_F22/VNN_CTRL
TP7075 — DT12 GPP_F23/V1P05_CTRL

(78,79) VCCAUX_VID0 — R7246 0_5%_2 — VCCAUX_VID0_R — DB37 GPP_B0/CORE_VID0
(78,79) VCCAUX_VID1 — R7247 0_5%_2 — VCCAUX_VID1_R — DB38 GPP_B1/CORE_VID1

VCCPRIM_1P8_1 CY18 1545mA — C7089 *1U/6.3V_4 — +1.8V_DEEP_SUS
VCCPRIM_1P8_2 CY20 — C7087 *1U/6.3V_4
VCCPRIM_1P8_3 CY24
VCCPRIM_1P8_4 CY26
VCCPRIM_1P8_5 DA18
VCCPRIM_1P8_6 DA20
VCCPRIM_1P8_7 DA22
VCCPRIM_1P8_8 DA24
VCCPRIM_1P8_9 DA26
VCCPRIM_1P8_10 DC18
VCCPRIM_1P8_11 DC20
VCCPRIM_1P8_12 DC22
VCCPRIM_1P8_13 DC24
VCCPRIM_1P8_14 DC26
VCCPRIM_1P8_15 DD20
VCCPRIM_1P8_16 DD22
VCCPRIM_1P8_17 DV22

R7238 *0_5%_6 — +3VPCU
R7229 0_5%_6 — +3V_DEEP_SUS

VCCPRIM_3P3_1 DA35 186mA +VCCPRIM_3P3
VCCPRIM_3P3_2 DC28 — C7272 *1U/6.3V_4
VCCPRIM_3P3_3 DC30 — C7273 *0.1U/16V_4
VCCPRIM_3P3_4 DD30

C7068 0.1u/16V_2 — 03/31 EE-16

DCPRTC DV34 — +VCCRTCEXT

VCCLDOSTD_0P85 DV46 +VCCLDOSTD_OUT_0P85 — C7299 2.2u/10V_4

Need GND gard

VCCA_CLKLDO_1P8_1 DV16 90mA VCCA_CLKLDO_1V8 — R7308 0_5%_4 — +1.8V_DEEP_SUS
VCCA_CLKLDO_1P8_2 DC15 — C7297 47u/6.3VS_6

VCCDPHY_1P24 DV28 22mA +VCCDPHY_1P24 — C7033 4.7U/6.3V_4
VCCDSW_1P05 DD38 3mA +VCCDSW_1P05 — C7059 1U/6.3V_4

VCC1P05_OUT_FET_1 BR3
VCC1P05_OUT_FET_2 BR4 — +VCC1.05_OUT_FET
VCC1P05_OUT_FET_3 BT5

VCCPRIM1P05_OUT_PCH_1 DA31 — 04/06 EE-29 R7002 1K_1%_4 — +VCC1.05_OUT_PCH
VCCPRIM1P05_OUT_PCH_2 DC33 — +BAT_RTC
VCCPRIM1P05_OUT_PCH_3 DC31 — C7001 1u/10V_2 — From Main BAT
C7004 0.1u/16V_2
C7000 *1U/6.3V_4

VCCRTC DC35 202mA +VCCRTC
VCCDSW_3P3 DD37 5mA VCCDSW_3P3
VCCPGPPR DA28 22mA — R7109 0_5%_2 — +1.8V_DEEP_SUS
R7103 *0_5%_2 — +3V_DEEP_SUS
R7231 0_5%_4 — +3VS5 — 04/06 EE-30
R7237 *0_5%_4 — +3VPCU

R7001 0_5%_4 — +3VS5
R7007 *0_5%_4 — +3VPCU
C7002 *1U/6.3V_4

For DSX/NDSX option
For DSX -->R7007
Non-DSX -->R7001

VCCPRIM_3P3_5 CY31 +VCCPFUSE_3P3
VCCPRIM_3P3_6 CY33 — R7237 *0_5%_4 — +3VPCU
VCCPRIM_1P8_18 CY39 — +1.8V_DEEP_SUS

RSVD_1 AP12 — AP12 — TP7021

TGL_U_IP_EXT/BGA

for DS3

+3VS5 — +3V_DEEP_SUS — **40mils**

R7245 *0_5%_6 — *Can't down size*

C7275 *1u/6.3V_2 — C7279 *0.1U/10V_2

+1.8V_DEEP_SUS
VCCAUX_VID0_R — R7259 *100K_5%_2
VCCAUX_VID1_R — R7260 *100K_5%_2

3V_S5

+3V_DEEP_SUS
R7290 100K_5%_2
VRALERT# — D7006 RB500V-40 — H_PROCHOT# (006,047,73,77)
R7279 *0_5%_2

BU2	**PROJECT : LS2B** Quanta Computer Inc.	
Size Custom	Document Number TGL-U 13/14(PCH POWER)	Rev 1A
Date: Friday, September 25, 2020	Sheet 016 of 105	

+3V (008,011,012,13,14,15,34,35,43,46,047,50,52,53,054,058,059,77,80,82)
+3VS5 (5,10,012,15,016,41,047,52,53,058,059,74,75,76,78,79,80)
+3V_DEEP_SUS (004,008,011,012,13,15,016,56,061,80)

	ID9
	1
	0

	ID8
	1
	0

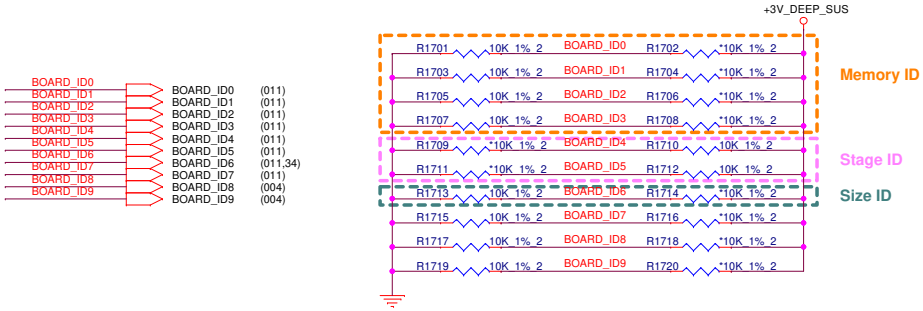
	ID7
	1
	0

	ID6
14 NON WOOFER	1
15 WOOFER	0

	ID5	ID4
EVT	0	0
SIT	0	1
SVT	1	1
SOVP	1	0

BOARD_ID[3:0]

ID3	ID2	ID1	ID0	
0	0	0	0	Samsung 8GB AKD5QGST514
0	0	0	1	Micron 8GB AKD5QGSTL24
0	0	1	0	Hynix 8GB AKD5QGSTW20
0	0	1	1	Reverse
0	1	0	0	Samsung 16GB AKD5RGUT503
0	1	0	1	Micron 16GB AKD5RGSTL05
0	1	1	0	Hynix 16GB AKD5RGUTW16
0	1	1	1	Reverse
1	0	0	0	Micron 16GB AKD5RGSTL05
1	0	0	1	Reverse
1	0	1	0	Reverse
1	1	1	1	Reverse
1	1	0	0	Reverse
1	1	0	1	Reverse
1	1	1	0	Reverse
1	1	1	1	Reverse



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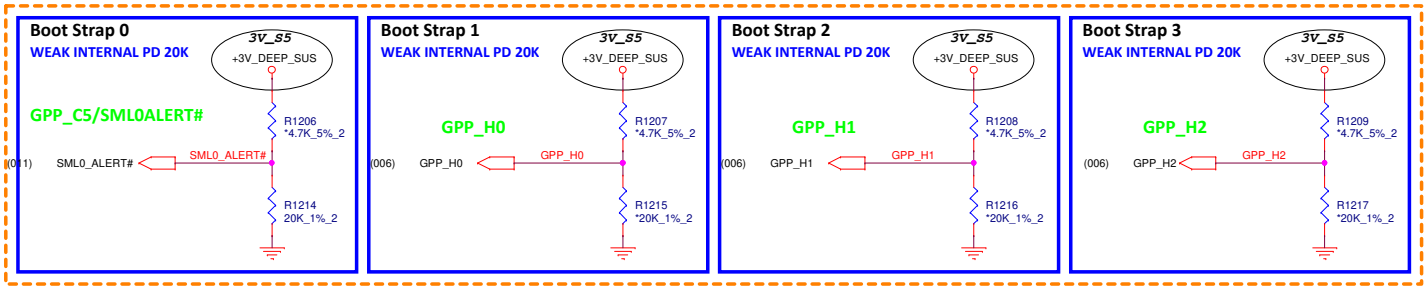
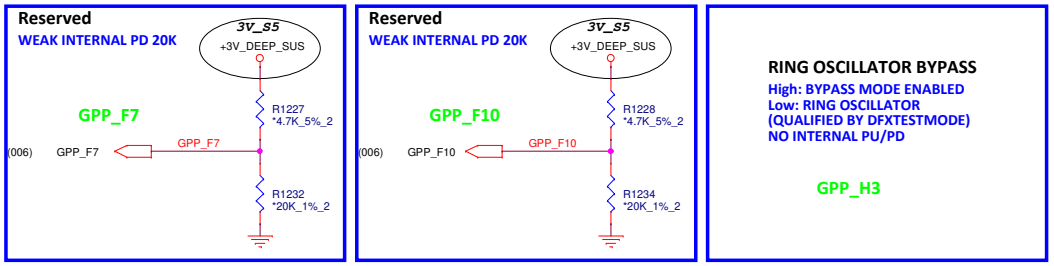


Boot Strap	4-bit boot strap configuration encodings
0000	BIOS/CSME on SPI & eSPI is enabled
0010	BIOS/CSME on SPI & eSPI is disabled
0100	BIOS on eSPI Peripheral Channel; CSME on master SPI
1000	BIOS/CSME on eSPI
1100	BIOS on eSPI peripheral Channel; CSME on slave SPI



BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CURRENT SENSOR-1	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CURRENT SENSOR-2	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CURRENT SENSOR-3	1A

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TBD
Slave Addresses:1001000 Placed close to
INA1_SCL/SDA

TBD
Slave Addresses:1001001 Placed close to
INA1_SCL/SDA

TBD
Slave Addresses:1001010 Placed close to
INA1_SCL/SDA

TBD
Slave Addresses:1001011 Placed close to
INA1_SCL/SDA

TBD
Slave Addresses:1001100 Placed close to
INA1_SCL/SDA

TBD
Slave Addresses:1001101 Placed close to
INA1_SCL/SDA

TBD
Slave Addresses:1001110 Placed close to
INA1_SCL/SDA

TBD
Slave Addresses:1001111 Placed close to
INA1_SCL/SDA

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TBD
Slave Addresses:1000000 Placed close to
INB0_SCL/SDA

TBD
Slave Addresses:1000001 Placed close to
INB0_SCL/SDA

TBD
Slave Addresses:1000010 Placed close to
INB0_SCL/SDA

TBD
Slave Addresses:1000011 Placed close to
INB0_SCL/SDA

TBD
Slave Addresses:1000100 Placed close to
INB0_SCL/SDA

TBD
Slave Addresses:1000101 Placed close to
INB0_SCL/SDA

TBD
Slave Addresses:1000110 Placed close to
INB0_SCL/SDA

TBD
Slave Addresses:1000111 Placed close to
INB0_SCL/SDA

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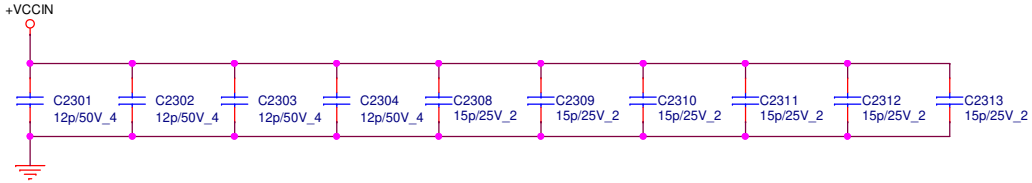
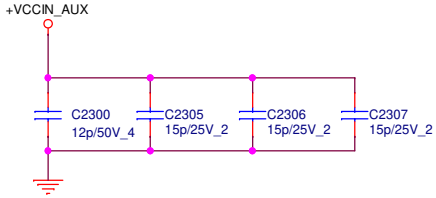
Table 7. INA231 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V_S	1000001
GND	SDA	1000010
GND	SCL	1000011
V_S	GND	1000100
V_S	V_S	1000101
V_S	SDA	1000110
V_S	SCL	1000111
SDA	GND	1001000
SDA	V_S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_S	1001101
SCL	SDA	1001110
SCL	SCL	1001111

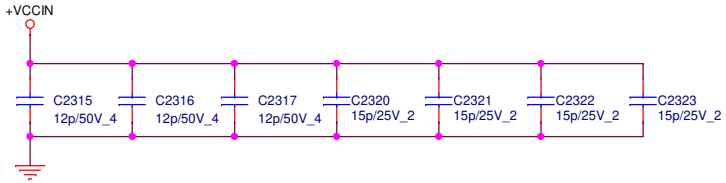
RF

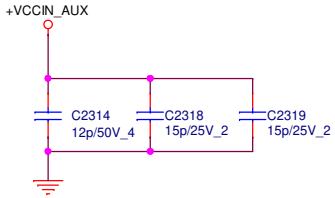
TOP Layer



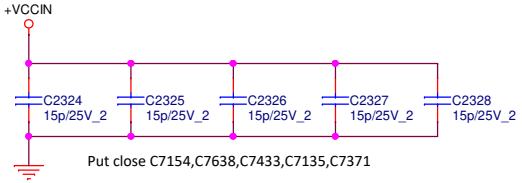


BOT Layer

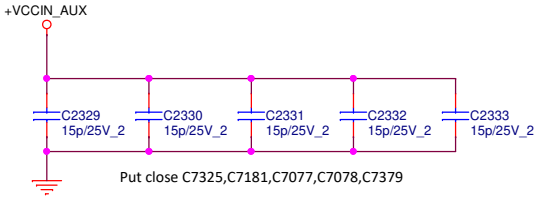




EMI



Put close C7154,C7638,C7433,C7135,C7371



Put close C7325,C7181,C7077,C7078,C7379

BU2	**PROJECT : LS2B** Quanta Computer Inc.	
Size B	Document Number **EMI / RF Caps**	Rev 1A
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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH /NC	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	PCH8	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	PCH9	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH STRAP	1A

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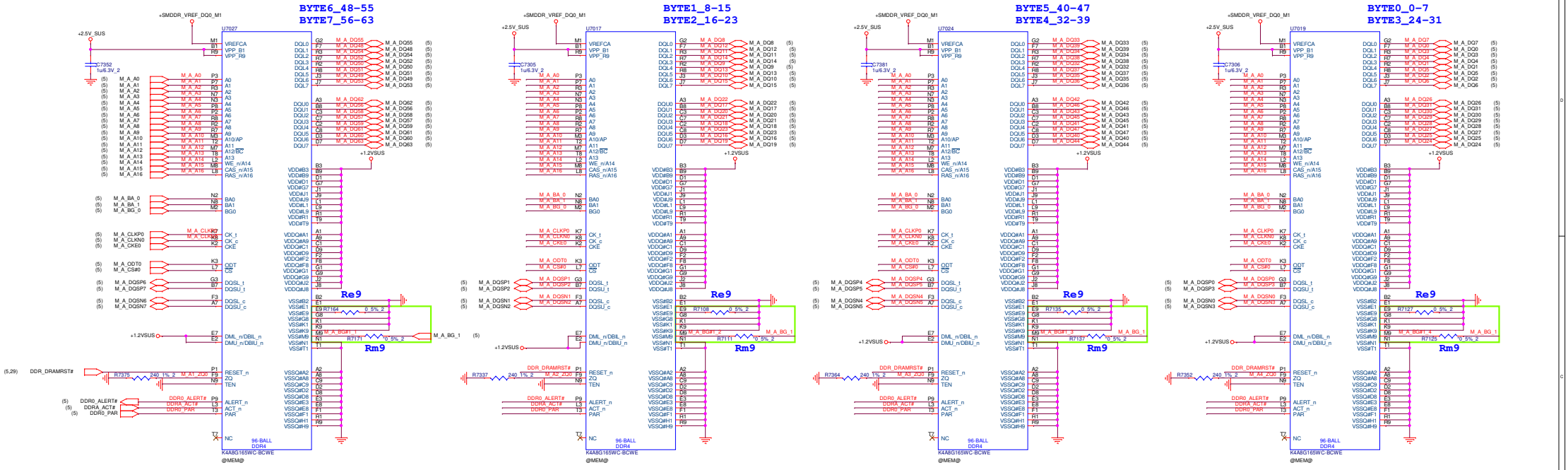
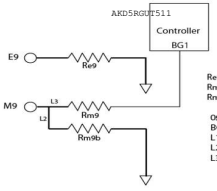
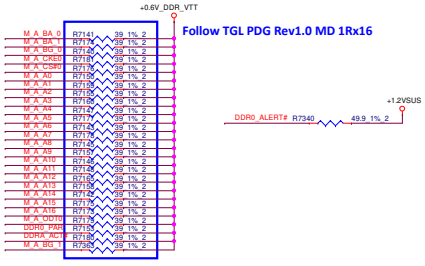


Vendor	Quanta P/N(VOL)	Quanta P/N(QCI)	Vendor P/N	SDP/DDP
Hynix 8Gb	AKD5QGSTW24	AKD5QGSTW20	H5AN8G6NCJR-XNC	SDP
Micron 8Gb	AKD5QGSTL27	AKD5QGSTL24	MT40A512M16TB-062E:J	SDP
Samsung 8Gb	AKD5QGST517	AKD5QGST514	K4A8G165WC-BCWE	SDP
Hynix 16Gb	AKD5RGUTW20	AKD5RGUTW16	H5ANAG6NCMR-XNC	DDP
Micron 16Gb	AKD5RGSTL07	AKD5RGSTL05	MT40A1G16KD-062E:E	SDP
Samsung 16Gb	AKD5RGUT510	AKD5RGUT503	K4AAG165WA-BCWE	SDP



	SDP x16	DDP x16
Re9	0Ω	240Ω
Rm9	open	0Ω
Rm9b	0Ω	open

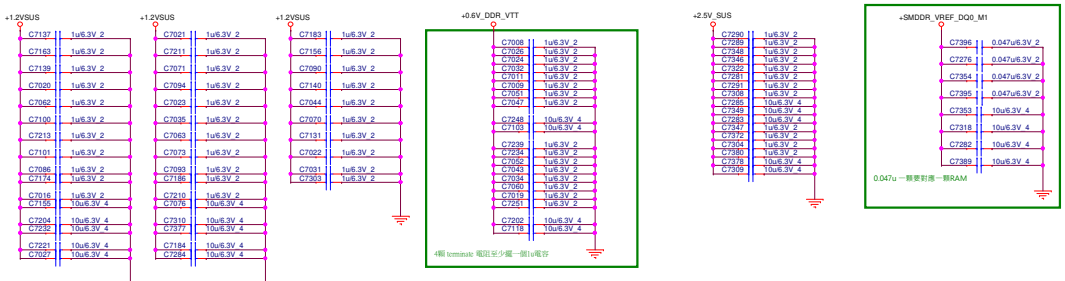
0Ω resistors should be low ESL
BG1 should be approx 5ps shorter
L1 < 0.1mm
L2 < 0.25mm
L3 < 2mm



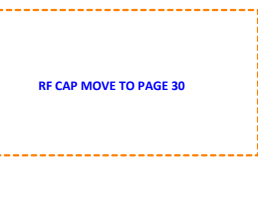
		SDP	DDP
E9 (Re9)	R7108	0Ω CS00001JE18	240Ω CS12401FE00
	R7127	0Ω CS00001JE18	240Ω CS12401FE00
	R7135	0Ω CS00001JE18	240Ω CS12401FE00
	R7164	0Ω CS00001JE18	240Ω CS12401FE00
M9 (Rm9)	R7111	UNINSTAL	0Ω CS00001JE18
	R7125	UNINSTAL	0Ω CS00001JE18
	R7137	UNINSTAL	0Ω CS00001JE18
	R7171	UNINSTAL	0Ω CS00001JE18
M9 (Rm9b)	R7110	0Ω CS00001JE18	UNINSTAL
	R7126	0Ω CS00001JE18	UNINSTAL
	R7138	0Ω CS00001JE18	UNINSTAL
	R7172	0Ω CS00001JE18	UNINSTAL

Memory 8Gbx16 & Memory 16Gbx16 TABLE

Place these Caps near Channel A Memory



RF CAP MOVE TO PAGE 30



VREF DQ0 M1 Solution

PROJECT : LS2B
Quanta Computer Inc.
BU2
Size: Custom | Document Number: On board DDR4 DIMM0 | Rev: 1A
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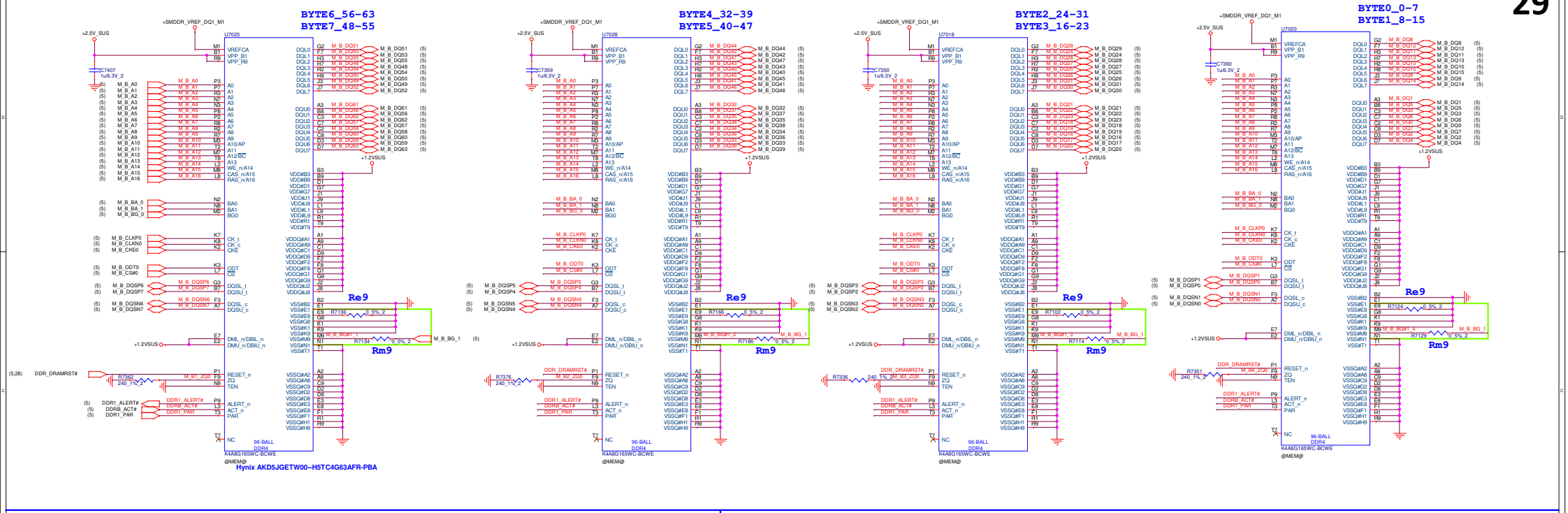
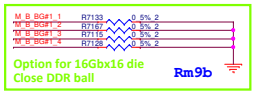
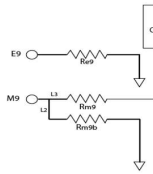


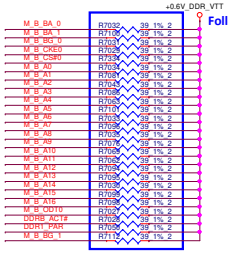
Vendor	Quanta P/N(VOL)	Quanta P/N(QCI)	Vendor P/N	SDP/DDP
Hynix 8Gb	AKD5QGSTW24	AKD5QGSTW20	H5AN8G6NCJR-XNC	SDP
Micron 8Gb	AKD5QGSTL27	AKD5QGSTL24	MT40A512M16TB-062E:J	SDP
Samsung 8Gb	AKD5QGST517	AKD5QGST514	K4A8G165WC-BCWE	SDP
Hynix 16Gb	AKD5RGUTW20	AKD5RGUTW16	H5ANAG6NCMR-XNC	DDP
Micron 16Gb	AKD5RGSTL07	AKD5RGSTL05	MT40A1G16KD-062E:E	SDP
Samsung 16Gb	AKD5RGUT510	AKD5RGUT503	K4AAG165WA-BCWE	SDP





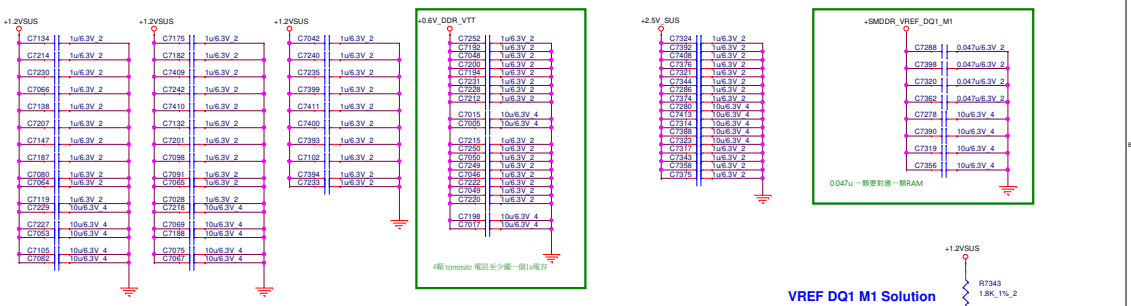
	SDP x16	DDP x16
Re9	0Ω	240Ω
Rm9	open	0Ω
Rm9b	0Ω	open

0Ω resistors should be low ESL
BG1 should be approx 5ps shorter
L1 < 0.1mm
L2 < 0.25mm
L3 < 2mm

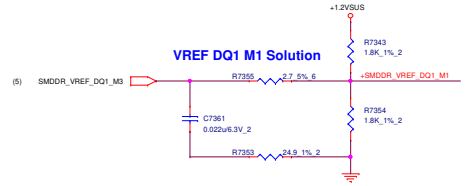


	Memory 8Gbx16 & Memory 16Gbx16 TABLE		
		SDP	DDP
E9 (Re9)	R7102	0Ω CS00001JE18	240Ω CS12401FE00
	R7124	0Ω CS00001JE18	240Ω CS12401FE00
	R7136	0Ω CS00001JE18	240Ω CS12401FE00
	R7166	0Ω CS00001JE18	240Ω CS12401FE00
M9 (Rm9)	R7114	UNINSTAL	0Ω CS00001JE18
	R7129	UNINSTAL	0Ω CS00001JE18
	R7134	UNINSTAL	0Ω CS00001JE18
	R7186	UNINSTAL	0Ω CS00001JE18
M9 (Rm9b)	R7115	0Ω CS00001JE18	UNINSTAL
	R7128	0Ω CS00001JE18	UNINSTAL
	R7133	0Ω CS00001JE18	UNINSTAL
	R7167	0Ω CS00001JE18	UNINSTAL

Place these Caps near Channel B Memory



RF CAP MOVE TO PAGE 30



+0.6V_DDR_VTT (28,30,75)
+1.2VSUS (5,7,9,28,30,75,82)
+2.5V_SUS (28,30,75)

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PROJECT : LS2B
Quanta Computer Inc.
BU2
Size: Custom | Document Number: On board DDR4 DIMM1 | Rev: 1A
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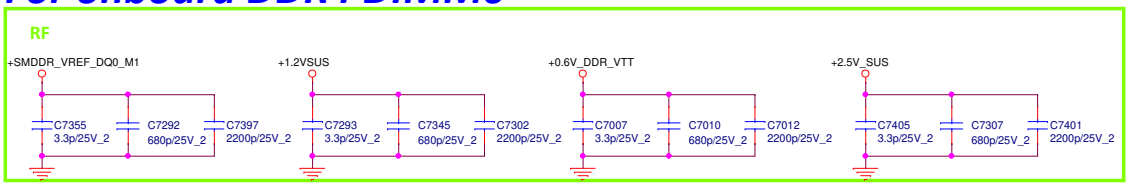
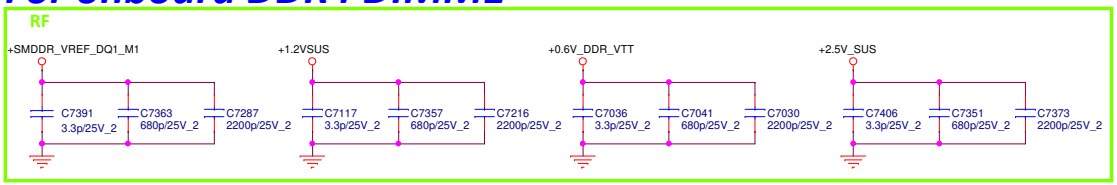
For onboard DDR4 DIMM0



For onboard DDR4 DIMM1



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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	MEMORY4	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	MEMORY5	1A

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Reserve

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BU2	PROJECT : LS2B Quanta Computer Inc.	
Size	Document Number System Power Enable /NC	Rev 1A
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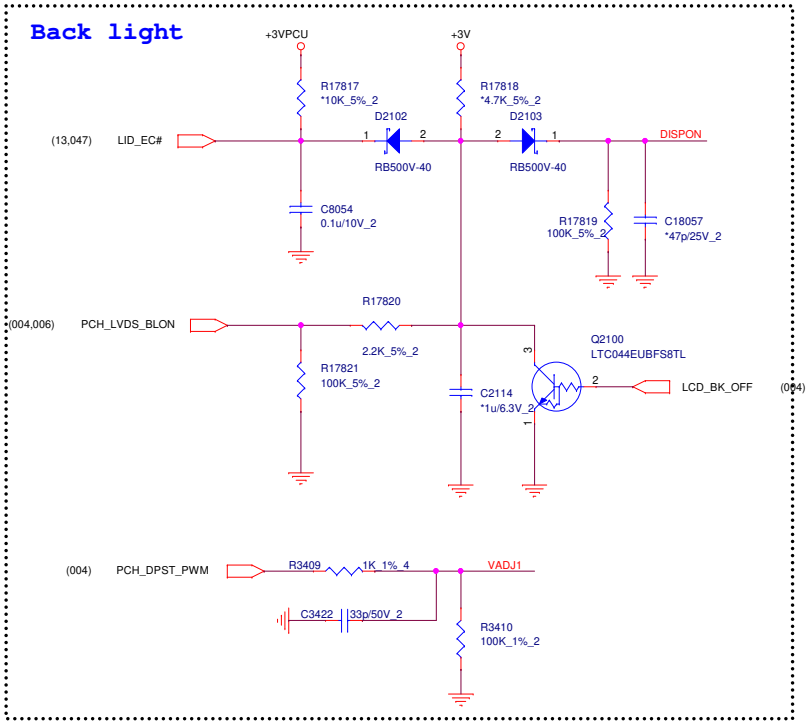
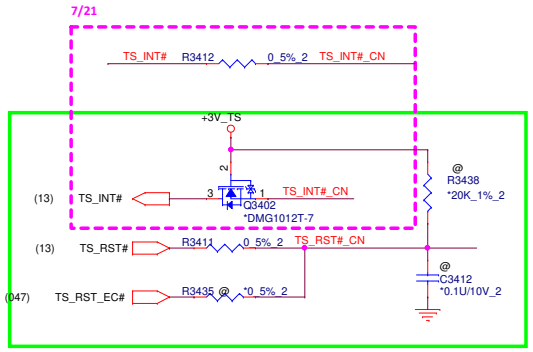
+3V (008,011,012,13,14,15,35,43,46,047,50,52,53,054,058,059,77,80,82)
+3VPCU (008,10,14,15,016,41,46,047,50,52,53,63,73,74,75,76,80)
+5V (35,36,047,50,054,80,82)
+VIN (50,73,74,75,76,77,78,81,82,83)

eDP Connector

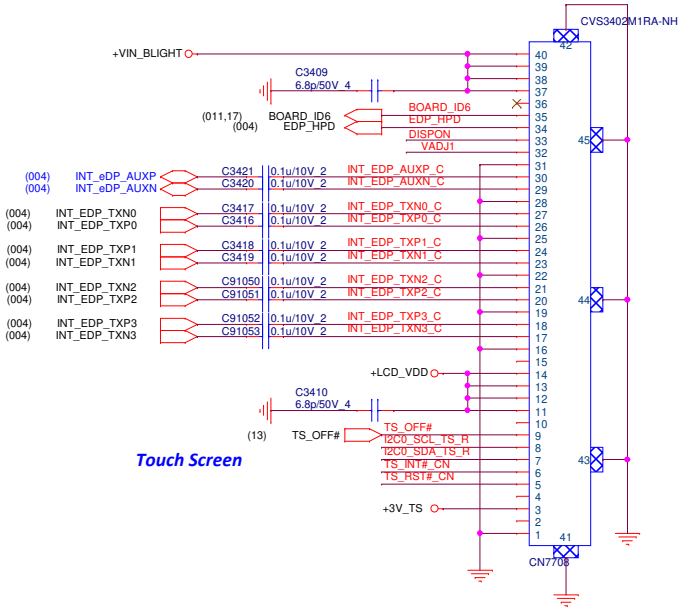
Back light



Nomal Touch Screen

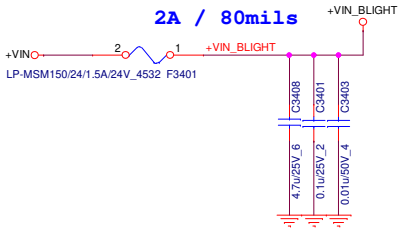


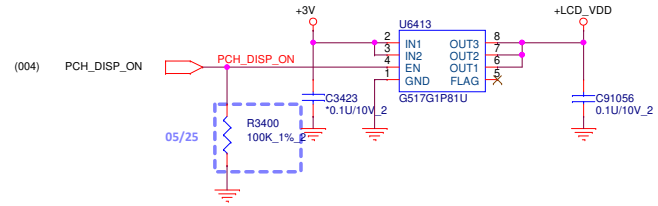
Panel

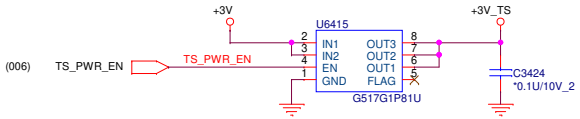


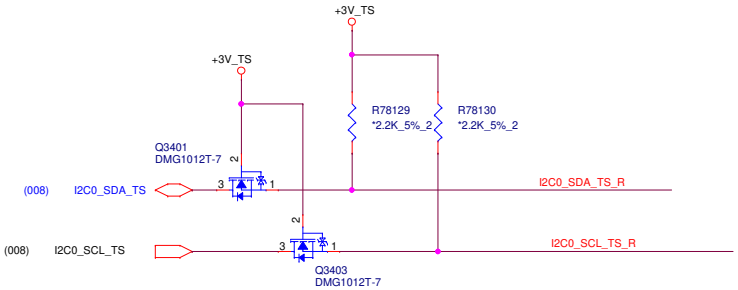
Touch Screen

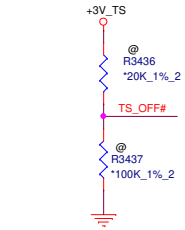
2A / 80mils



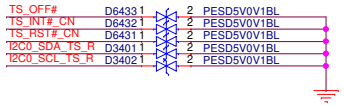








For Touch screen sequence Reserve



BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	eDP/TS	1A

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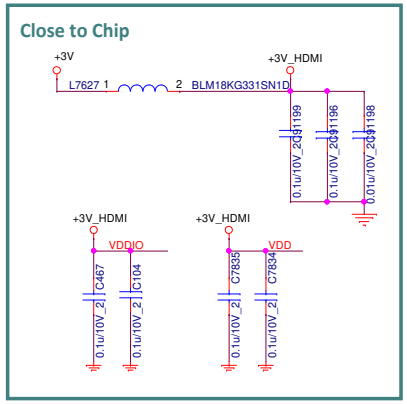
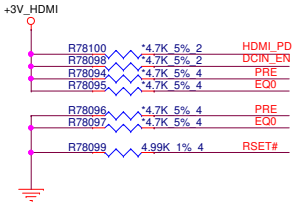
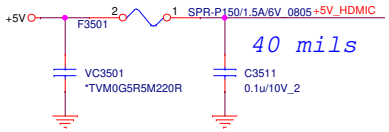
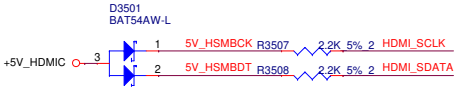
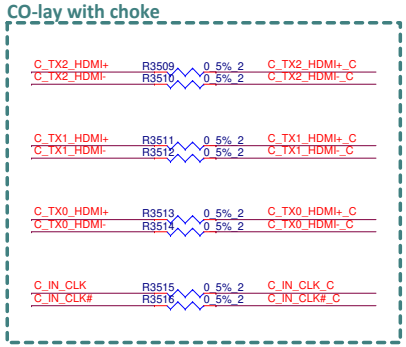
HDMI CONN

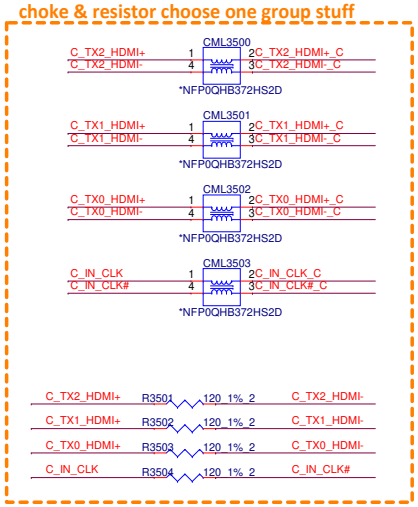


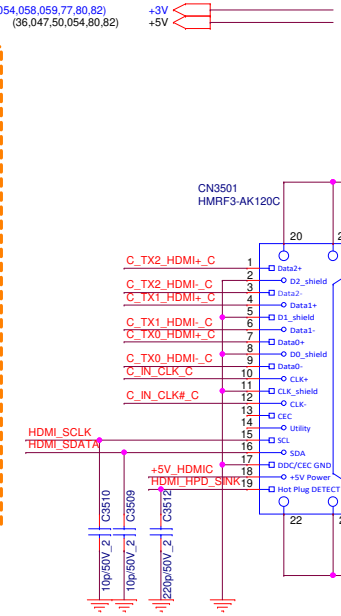


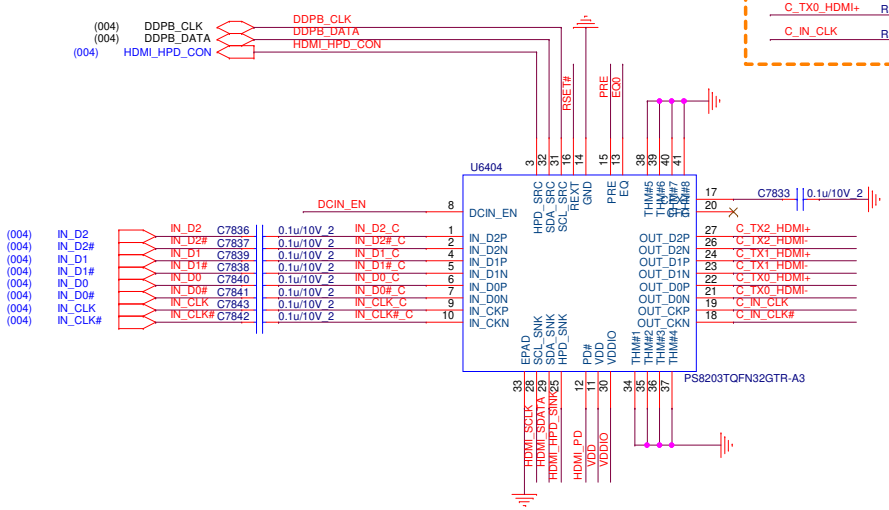




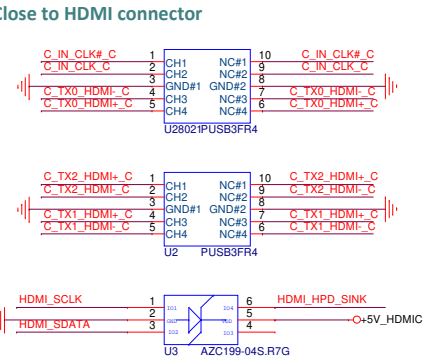








Internal Pull down 150K on HDMI_HPD_SNK



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BU2	PROJECT : LS2B Quanta Computer Inc.	
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ALC3306-CG

+5V (35,047,50,054,80,82)
+1.8V (15,037,46,80)

+1.8V_CODEC — L3603 BLM15PX181SN1D — +1.8V_DVDD
C3606 1u/6.3V_2
C3608 0.1u/10V_2

+1.8V, +1.8V_CODEC, R78139 *Short_0402, +5V, +5V_CODEC, R78140 *Short_0603 (8/28)

AGND SHIELD

AGND Plane | DGND Plane

+5V_AVDD >40mils trace

+5V_AVDD — L3601 BLM15PX181SN1D — +5V_CODEC
C3601 4.7u/6.3V_4 (7/29), C3602 0.1u/10V_2
Close to PIN40

+1.8V_AVDD — L3602 BLM15PX181SN1D — +1.8V_CODEC
C3604 2.2u/10V_4, C3605 0.1u/10V_2
Close to PIN20

BIT_CLK_AUDIO — C91203 *10p/50V_2

+5V_CODEC — L3604 UPB160808T-121Y-N — +5V_DVDD
C3617 4.7u/6.3V_4 (7/29), C3618 0.1u/10V_2
Close to PIN41

Close to PIN46
C3623 4.7u/6.3V_4 (7/29), C3624 0.1u/10V_2

Analog
Digital
Speaker 4 ohm: 40mils

ALC3306-CG

U3601

Pin	Signal	Net
36	PCBEEP	ALG_BEEP_IN
35	MIC2-CAP	AC54, C3621
34	MIC2-R/SLEEV	SLEEVE
33	MIC2-L/RING2	RING2
32	MIC2-VREFO-R	VREFOUT_R, R3611
31	MIC2-VREFO-L	VREFOUT_L, R3614
30	HPOUT-L	HPOUT_L
29	HPOUT-R	HPOUT_R
28	CPVPP	C3620 1u/10V_4, C8732 1u/10V_4
27	CBN1	C3619 1u/10V_4
26	CBP1	
25	CBP2	
24	CBN2	CBN2
23	CPVEE	CPVEE, C8733 1u/10V_4
22	AVSS2	AGND
21	LDO2_CAP	C3612 2.2u/10V_4
20	AVDD2	+1.8V_AVDD
19	LDO3_CAP	C3622 2.2u/10V_4
18	DVDD_IO	+1.8V_DVDD
17	SDATA_OUT	ACZ_SDOUT_AUDIO (15)
16	SDATA_IN	HD_SDIN0, R3605 33.2_1%_2, ACZ_SDIN0 (15)
15	SYNC	ACZ_SYNC_AUDIO (15)
14	BCLK	BIT_CLK_AUDIO (15)
13	GPIO3/JDET/EAPD	EAPD (037)
12	I2S_LRCLK	
11	I2S_MCLK	
10	I2S_BCLK	
9	I2S_DOUT	
8	I2S_DIN	
7	I2C_SCL	
6	I2C_SDA	
5	GPIO1/DMIC-CLK	
4	GPIO0/DMIC-DATA-12	
3	DVDD	+1.8V_DVDD
2	PDB	
1	SPDIFO/GPIO2/DMIC-DATA-34/I2S OE	
37	AVSS1	AGND
38	VREF	C3614 2.2u/10V_4, C3611 2.2u/10V_4
39	LDO1_CAP	
40	AVDD1	+5V_AVDD
41	PVDD1	+5V_DVDD
42	SPK-L+	L_SPK+
43	SPK-L-	L_SPK-
44	SPK-R-	R_SPK-
45	SPK-R+	R_SPK+
46	PVDD2	
47	JD1/HP_JD	HP_JD
48	JD2/GPIO2	
49	PAD	

+1.8V_DVDD — R3610 100K_1%_2 — HP_JD — R77905 200K_1%_2, C28099 *0.1u/10V_2
(36) HPOUT-JD
TP3601 HP_EAPD
PD#
(46) Audio_SDA_DMIC
(46) Audio_SCL_DMIC

+1.8V_DVDD — R3613 100K_1%_2
(047) VOLMUTE# — D3601 RB500V-40
PD#
C3626 0.1u/10V_2
(15) ACZ_RST#_AUDIO — R3615 *0_5%_2 — Q3601 *METR3904-G
R3616 *10K_1%_4 — +1.8V_DVDD

PC BEEP

R3820 AMP@0_5%_4 — I2S_LRCLK (037) (008,012,047)
R3821 AMP@0_5%_4 — MIC_LED#_A (50)
R3822 AMP@0_5%_4 — I2S_BCLK (037)
R3823 AMP@0_5%_4 — I2S_DOUT (037)
I2S_DIN (037)
I2C_SCL_AMP1, I2C_SDA_AMP1

Digital | Analog
ACZ_SPKR — AR23 10K_5%_2 — ALG_BEEPIN_B — ALG_BEEP_IN
AC19 *100p/50V_2
AR17 10K_5%_2

(46,047,054) MBCLK2 — R77993 *0_5%_4 — Q3604 *DMG1012T-7 — I2C_SCL_AMP — I2C_SCL_AMP (037)
I2C_SCL_AMP1 — R3618 AMP@0_5%_4

(46,047,054) MBDATA2 — R77992 *0_5%_4 — Q3603 *DMG1012T-7 — I2C_SDA_AMP — I2C_SDA_AMP (037)
I2C_SDA_AMP1 — R3619 AMP@0_5%_4

I2S_LRCLK, I2S_BCLK, I2S_DOUT, I2S_DIN
C3641 10P/50V_4, C3642 10P/50V_4, C3643 10P/50V_4, C3644 10P/50V_4

SPK CONN

Close to Speaker Speaker 4 ohm: 40mils

HPOUT_R R77810 30_1%_4, HPOUT_L R77809 30_1%_4
RING2 — L3605 BLM18KG121TN1D — HPOUT_R_C1 — L3606 BLM18KG121TN1D — HPOUT_R_C2 — MIC2_L
HPOUT_L_C1 — L3607 BLM18KG121TN1D — HPOUT_L_C2
HPOUT-JD — L3608 BLM18KG121TN1D — HPOUT-JD_R
SLEEVE — L3609 BLM18KG121TN1D — MIC2_R
CN3701 — 2SJ3127-008111F — AGND

SCHEMATIC

MIC2_L: C3640 1000p/50V_2, D6413 PESD5V0V1BL
MIC2_R: C3639 1000p/50V_2, D6414 PESD5V0V1BL
HPOUT_L_C2: C3638 1000p/50V_2, D6415 PESD5V0V1BL
HPOUT_R_C2: C3637 1000p/50V_2, D6416 PESD5V0V1BL
HPOUT-JD_R: C3636 1000p/50V_2, D6417 PESD5V0V1BL
AGND

HPOUT-JD — HPOUT-JD (36)

L_SPK+, L_SPK-, R_SPK-, R_SPK+ — CN7713 50207-00471-001

EC3602 0_5%_4, EC3603 1000P/50V_4, EC3604 0_5%_4 — AGND
R3617 0_5%_4, R77967 0_5%_4, R77968 0_5%_4, R77969 0_5%_4 — AGND

6/25

L_SPK+ — C3631 1000p/50V_2 — D30 PESD5V0V1BL
L_SPK- — C3632 1000p/50V_2 — D31 PESD5V0V1BL
R_SPK+ — C3634 1000p/50V_2 — D32 PESD5V0V1BL
R_SPK- — C3633 1000p/50V_2 — D33 PESD5V0V1BL

BU2

PROJECT : LS2B
Quanta Computer Inc.

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	Codec ALC3306	1A

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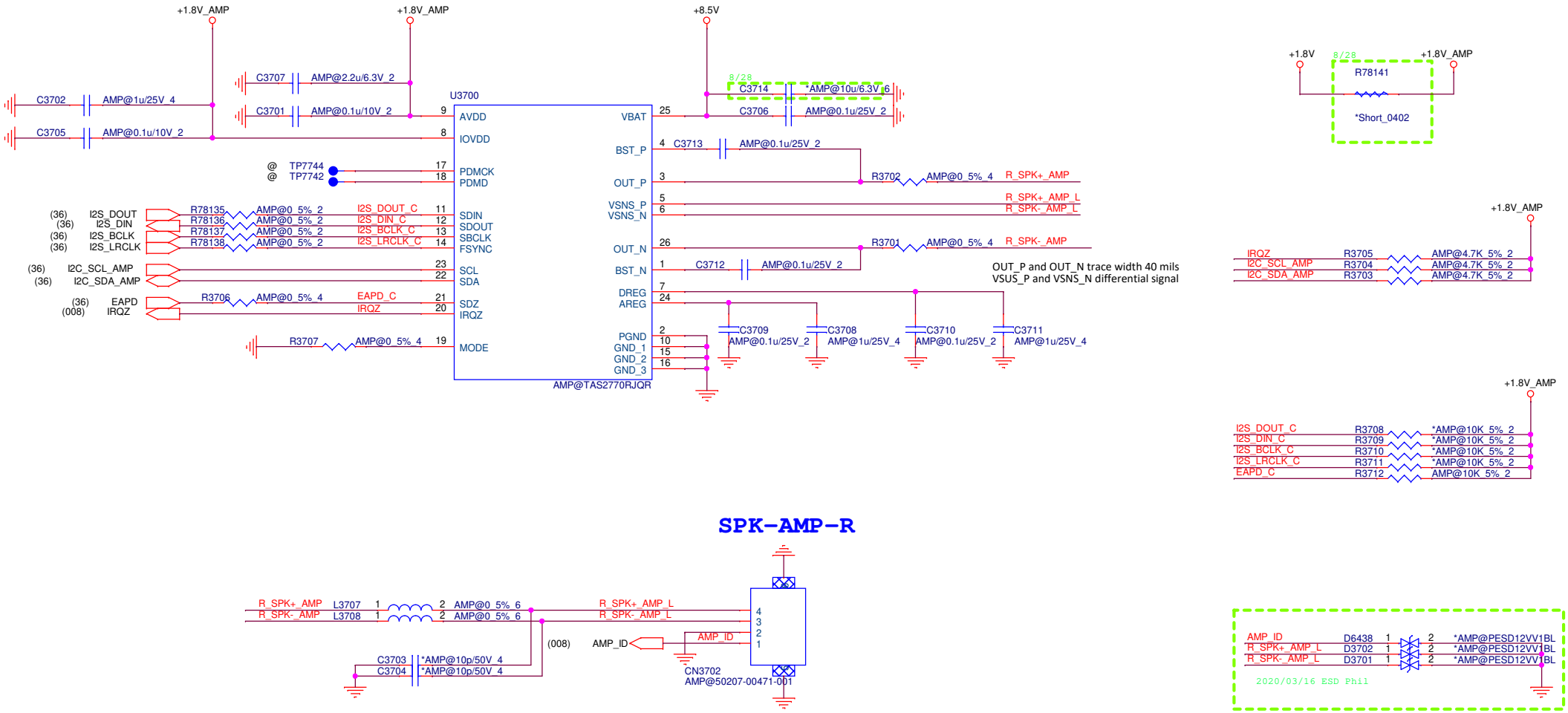
(34,50,73,74,75,76,77,78,81,82,83) +VIN
(008,011,012,13,14,15,34,35,43,46,047,50,52,53,054,058,059,77,80,82) +3V
(15,36,46,80) +1.8V
(81,82) +8.5V



SPK-AMP-R

BU2	PROJECT :LS2B Quanta Computer Inc.	
Size	Document Number SPEAKER AMP-TAS2770	Rev 1A
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Reserve

Reserve

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	Headphone /NC	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	LAN / RJ45 /NC	1A

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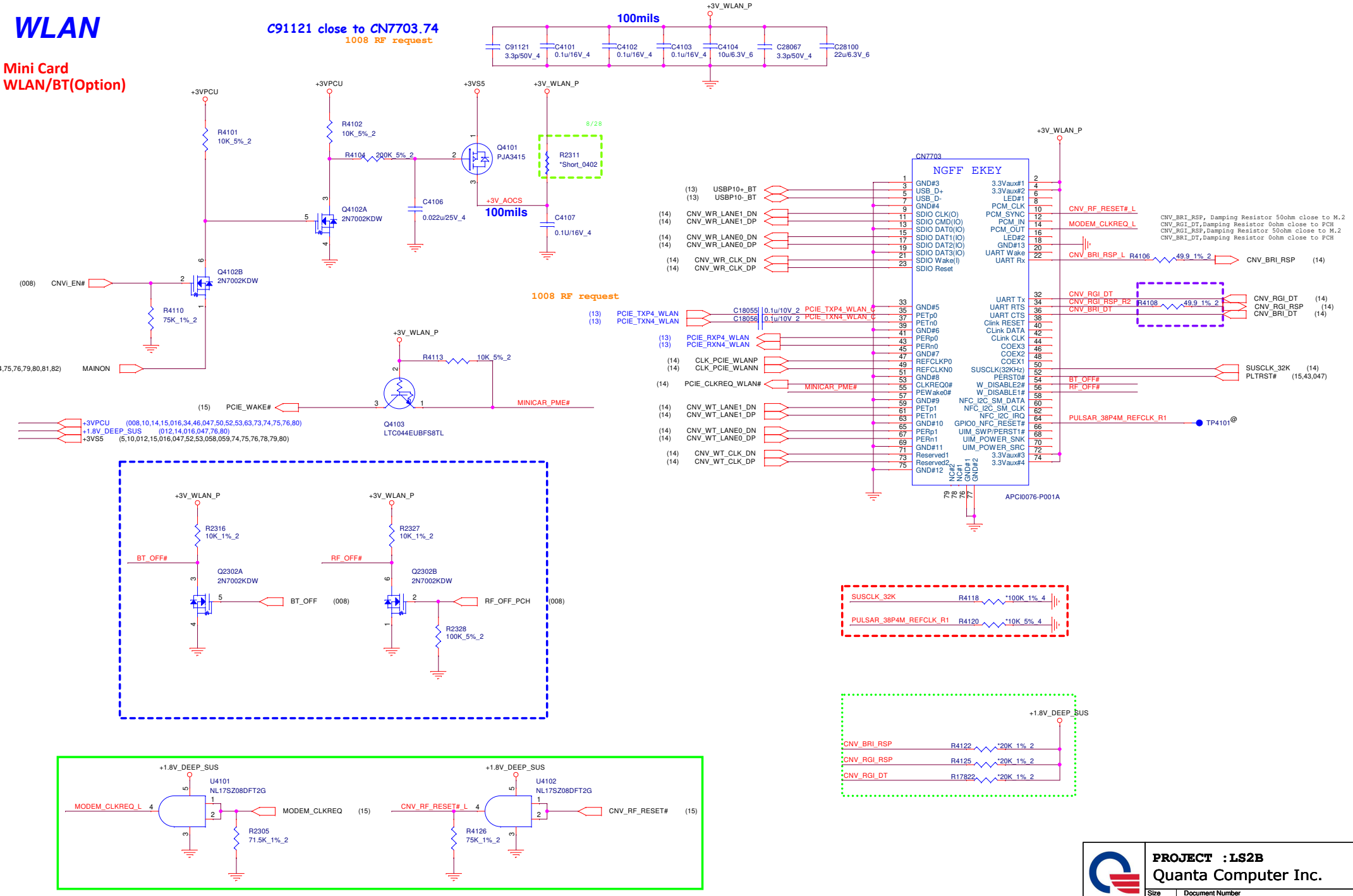
WLAN

C91121 close to CN7703.74
1008 RF request

Mini Card
WLAN/BT(Option)



BU2	PROJECT : LS2B Quanta Computer Inc.	
Size	Document Number NGFF WLAN E Key	Rev 1A
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WWAN

Reserve

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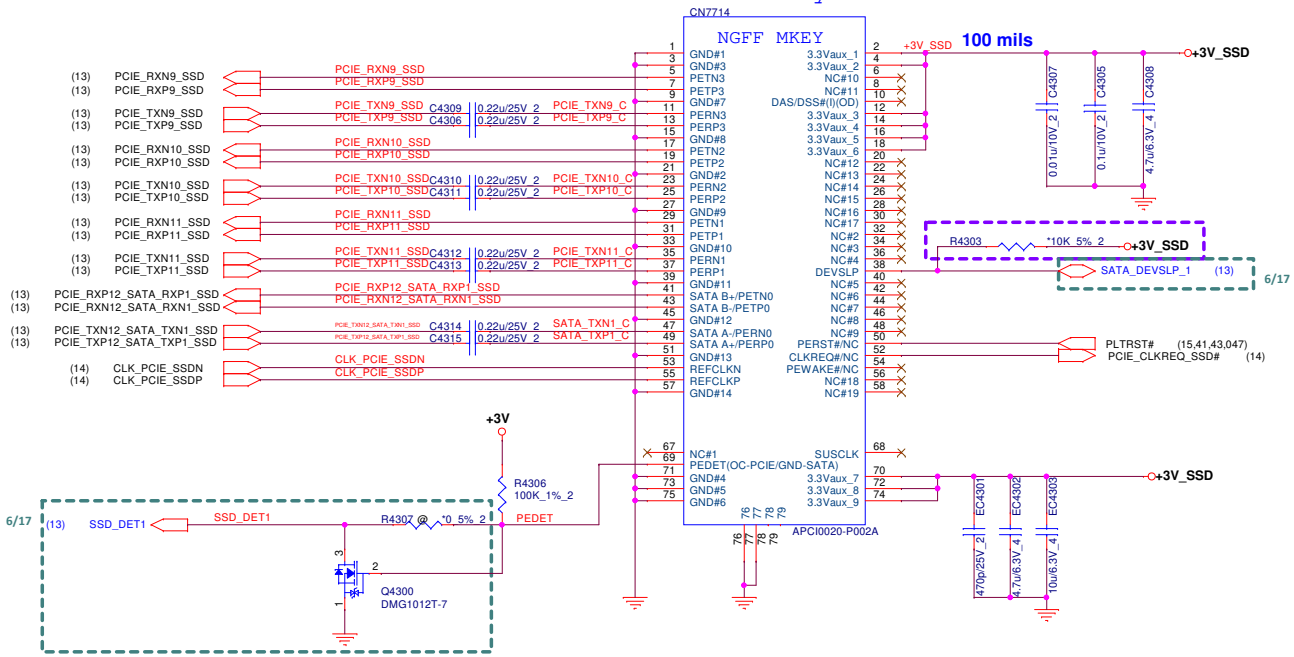
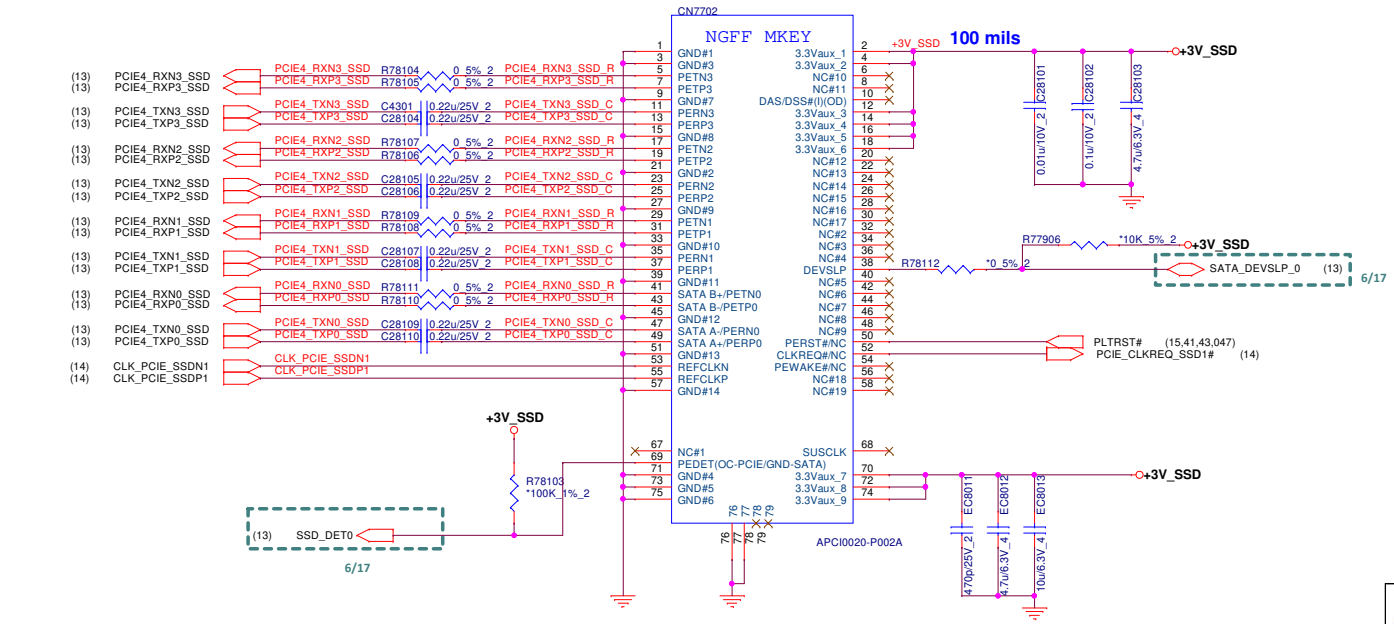
SATA SSD

(80) +3V_SSD

2242 M key



2280 M key



BU2	PROJECT : LS2B Quanta Computer Inc.	
	Size / Document Number: NGFF SSD M Key	Rev 1A
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BU2

PROJECT : LS2B

Quanta Computer Inc.

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	HDD / ODD /NC	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	eMMC /NC	1A

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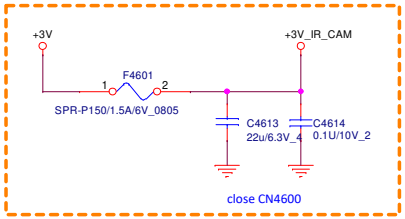
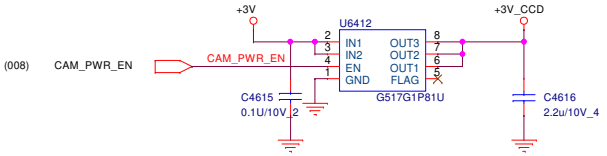
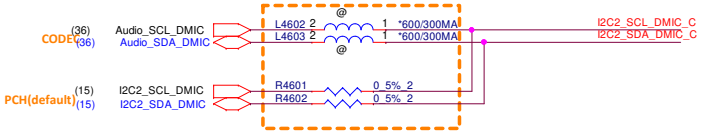
IR CAM PWR



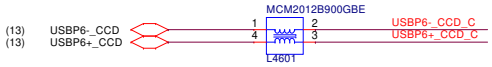
IR CAM PWR For SFH4770S

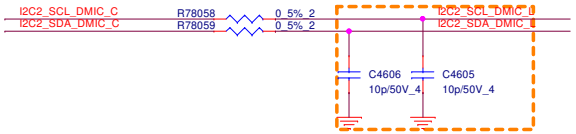




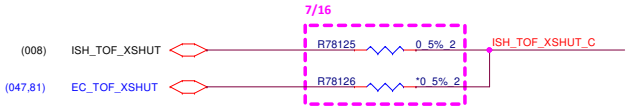
Place together

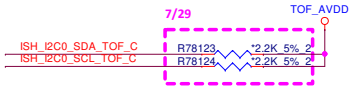
Webcam

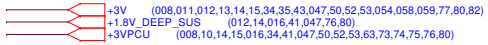




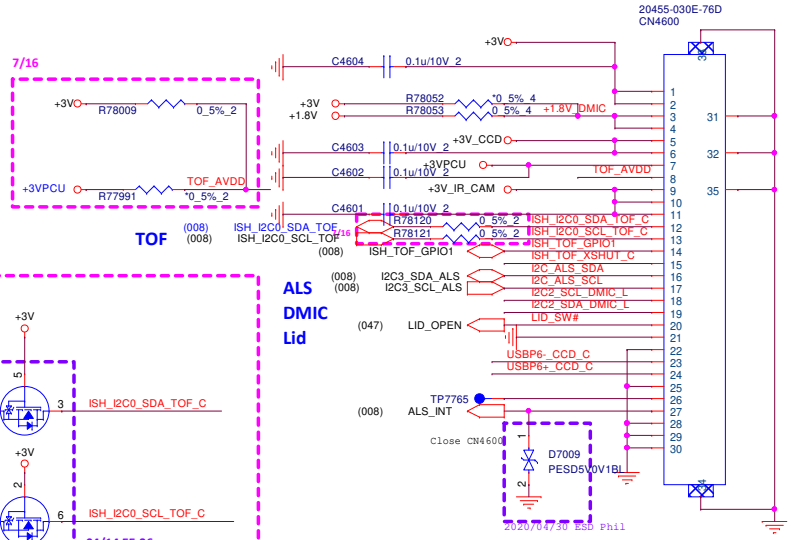
Close CN4600







CAMERA CONN



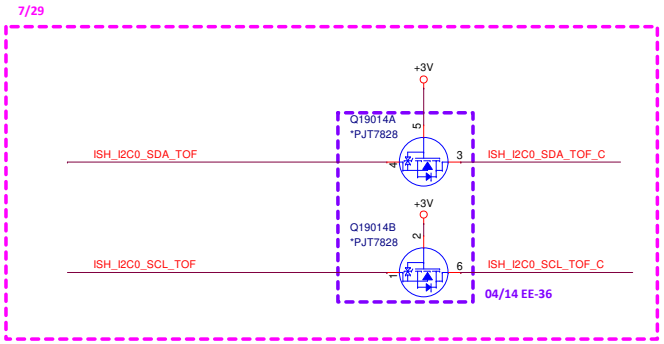
TOF

ALS

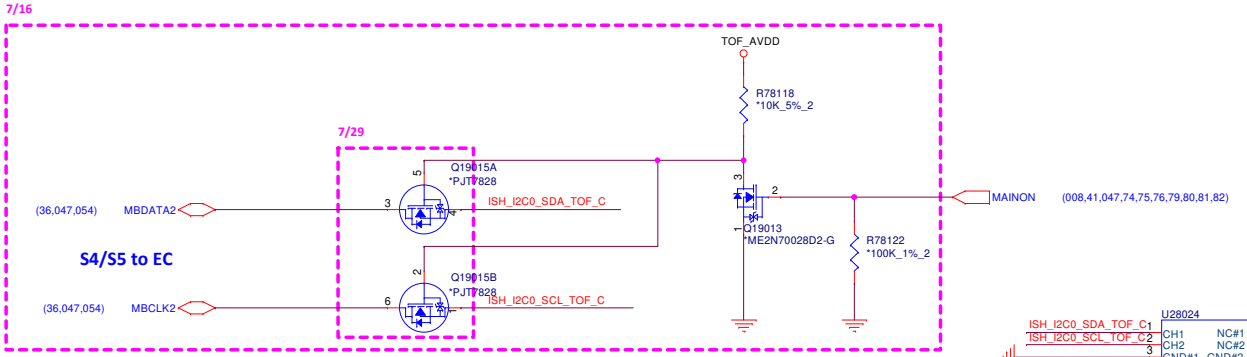
DMIC

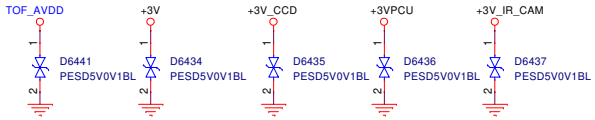
Lid

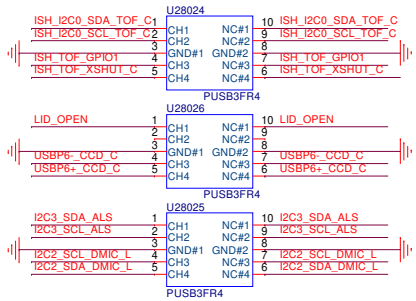
S0 to PCH



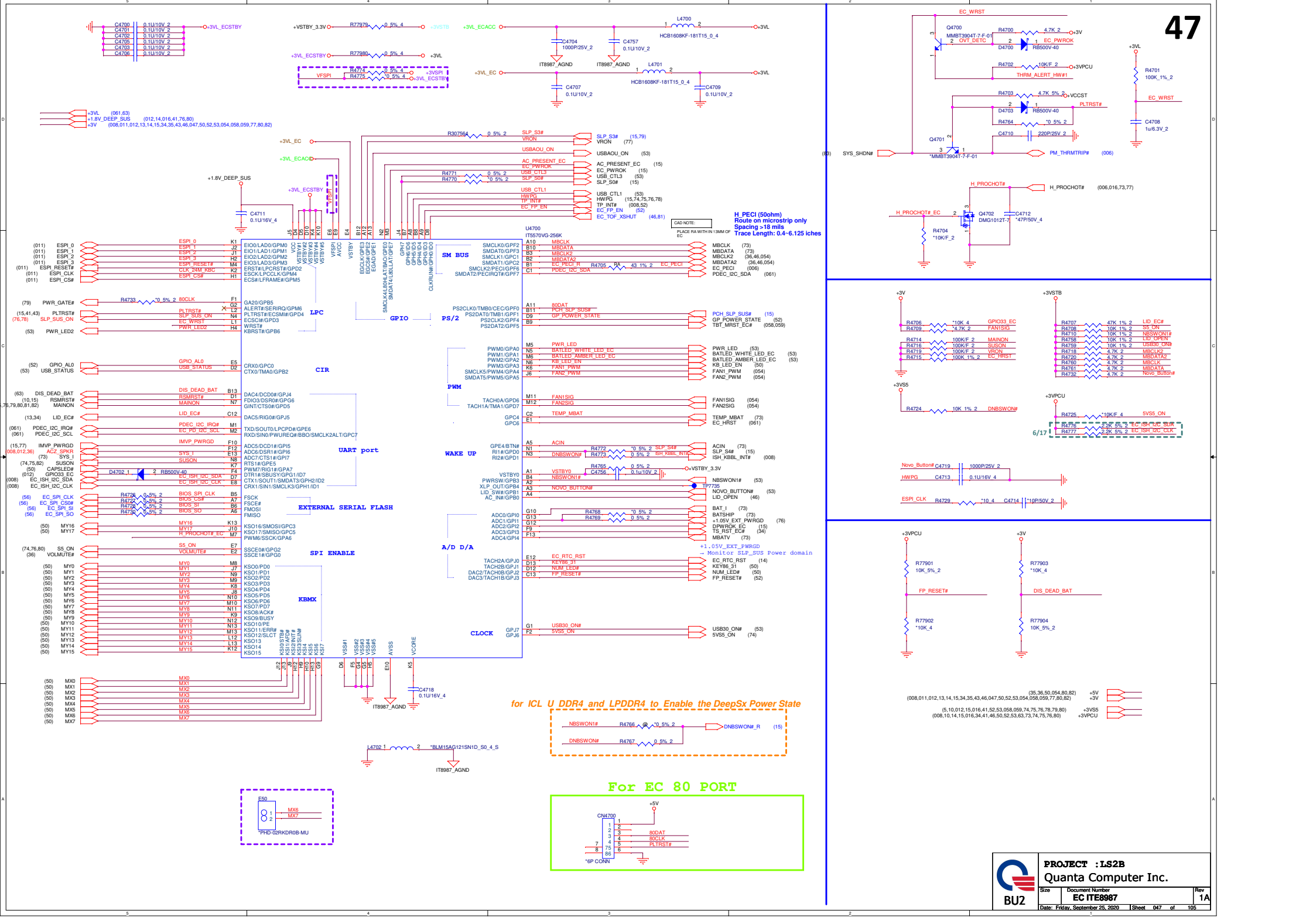
S4/S5 to EC







BU2	PROJECT : LS2B Quanta Computer Inc.	
Size	Document Number CAM/ALS/TOF	Rev 1A
Date: Friday, September 25, 2020	Sheet 46 of 105	


U4700
IT5570VG-256K
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
CAD NOTE:
PLACE RA WITH IN 13MM OF EC
for ICL U DDR4 and LPDDR4 to Enable the DeepSx Power State
For EC 80 PORT
CN4700
*6P CONN
E50
*PHD-02RKDR0B-MU
PROJECT :LS2B
Quanta Computer Inc.
BU2
EC ITE8987
Rev 1A
Date: Friday, September 25, 2020
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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	EC /NC	1A

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Reserve

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BU2

PROJECT : LS2B

Quanta Computer Inc.

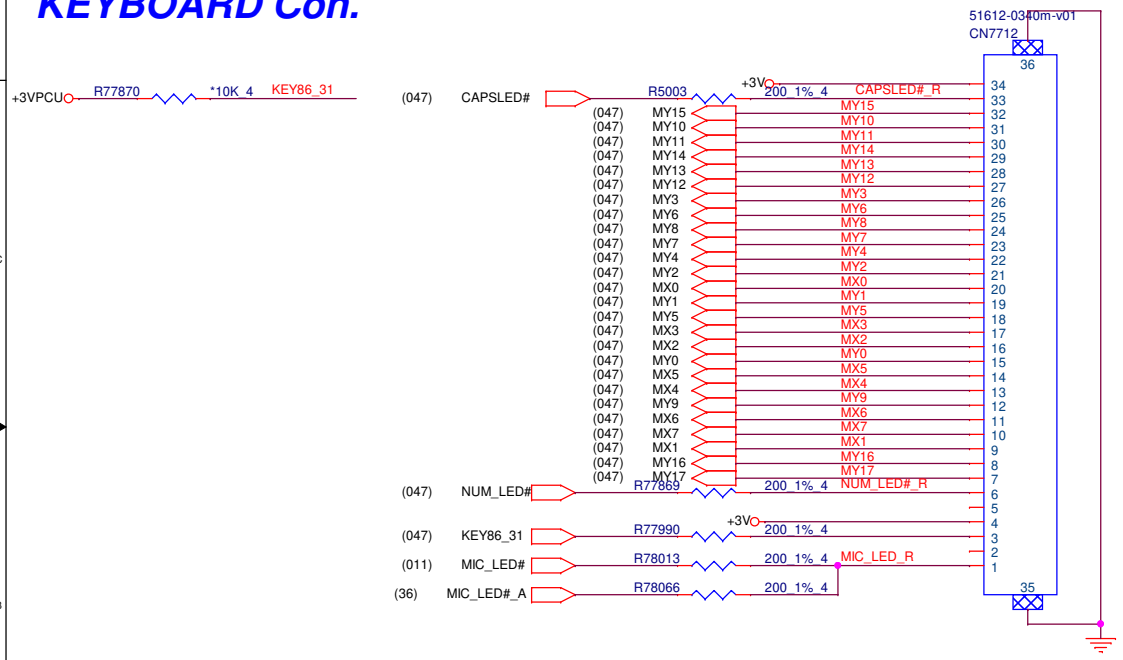
Size	Document Number	Rev
	EC /NC	1A

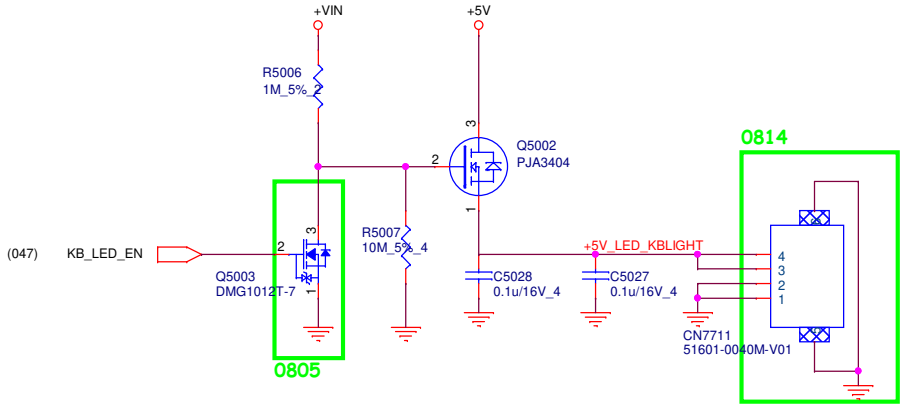
Date: Friday, September 25, 2020 Sheet 49 of 84

KB LIGHT CONN (14")

+3VS5 (5,10,012,15,016,41,047,52,53,058,059,74,75,76,78,79,80)
+3V (008,011,012,13,14,15,34,35,43,46,047,52,53,054,058,059,77,80,82)
+5VS5 (15,52,53,061,74,75,76,77,78,79,80)

KEYBOARD Con.





MY0	C5011	220p/50V_2
MY1	C5002	220p/50V_2
MY2	C5005	220p/50V_2
MY3	C5007	220p/50V_2
MY4	C5008	220p/50V_2
MY5	C5001	220p/50V_2
MY6	C5004	220p/50V_2
MY7	C5010	220p/50V_2
MY8	C5013	220p/50V_2
MY9	C5016	220p/50V_2
MY10	C5019	220p/50V_2
MY11	C5022	220p/50V_2
MY12	C5015	220p/50V_2
MY13	C5018	220p/50V_2
MY14	C5021	220p/50V_2
MY15	C5024	220p/50V_2
MY16	C5025	220p/50V_2
MY17	C5026	220p/50V_2
MX0	C5006	220p/50V_2
MX1	C5012	220p/50V_2
MX2	C5023	220p/50V_2
MX3	C5020	220p/50V_2
MX4	C5014	220p/50V_2
MX5	C5009	220p/50V_2
MX6	C5017	220p/50V_2
MX7	C5003	220p/50V_2

KEYBOARD PULL-UP

+3VPCU

R100	*8.2K_5%_2	MY0
R101	*8.2K_5%_2	MY1
R102	*8.2K_5%_2	MY2
R103	*8.2K_5%_2	MY3
R104	*8.2K_5%_2	MY4
R105	*8.2K_5%_2	MY5
R106	*8.2K_5%_2	MY6
R107	*8.2K_5%_2	MY7
R108	*8.2K_5%_2	MY8
R109	*8.2K_5%_2	MY9
R110	*8.2K_5%_2	MY10
R111	*8.2K_5%_2	MY11
R112	*8.2K_5%_2	MY12
R113	*8.2K_5%_2	MY13
R114	*8.2K_5%_2	MY14
R115	*8.2K_5%_2	MY15
R116	*8.2K_5%_2	MY16
R117	*8.2K_5%_2	MY17

BU2

PROJECT : LS2B
Quanta Computer Inc.

Size	Document Number	Rev
	Kerboard/Keyboard Backlight	1A

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BU2

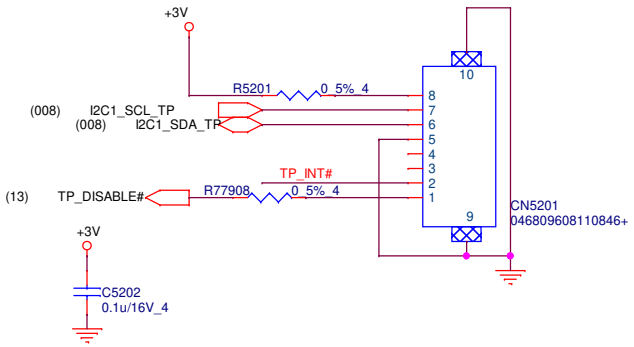
PROJECT : LS2B

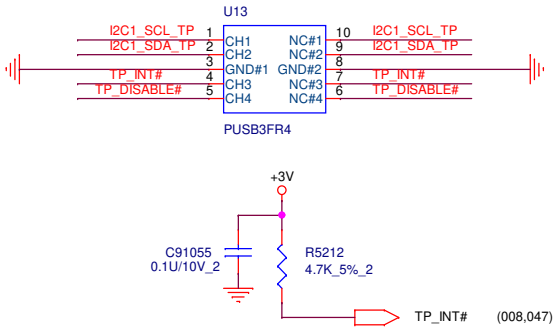
Quanta Computer Inc.

Size	Document Number	Rev
	TPM/NC	1A

Date: Friday, September 25, 2020 | Sheet 51 of 84

Touch Pad





Finger print

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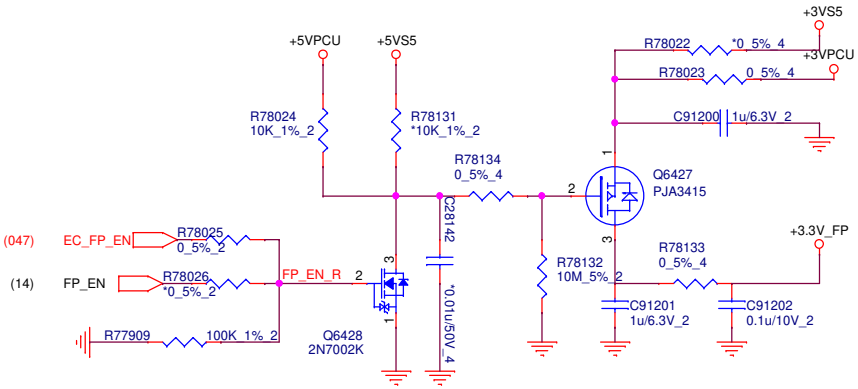
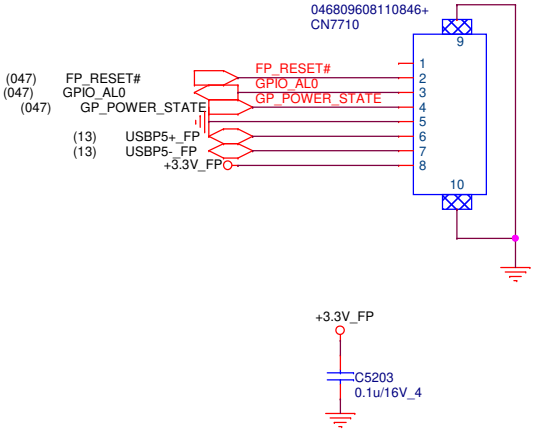
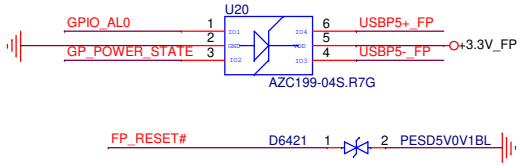
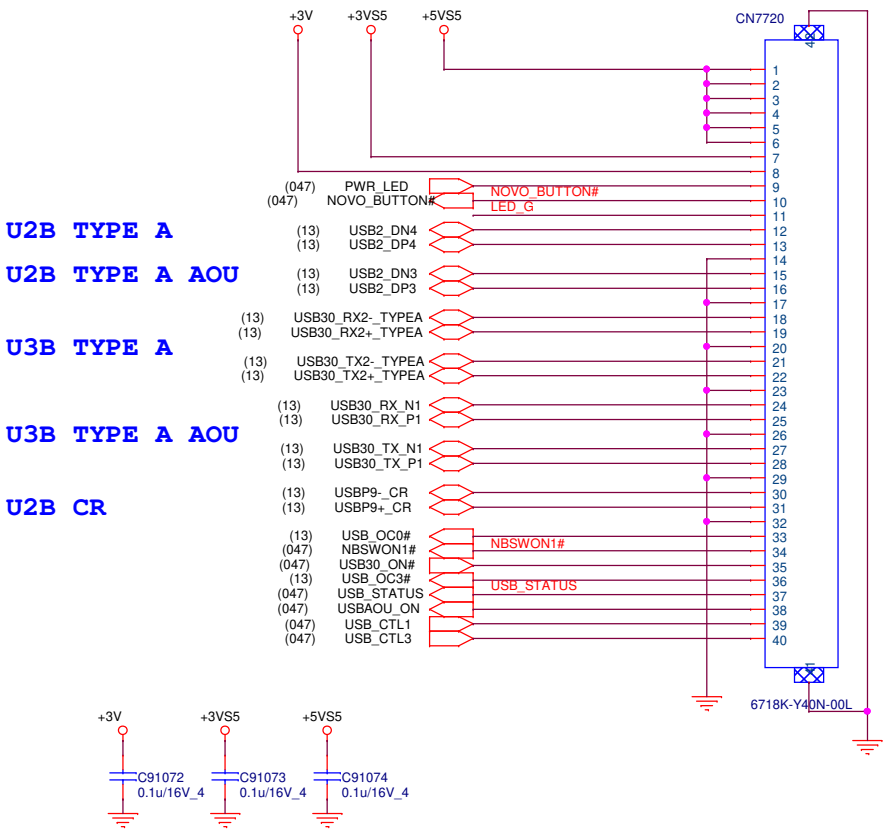


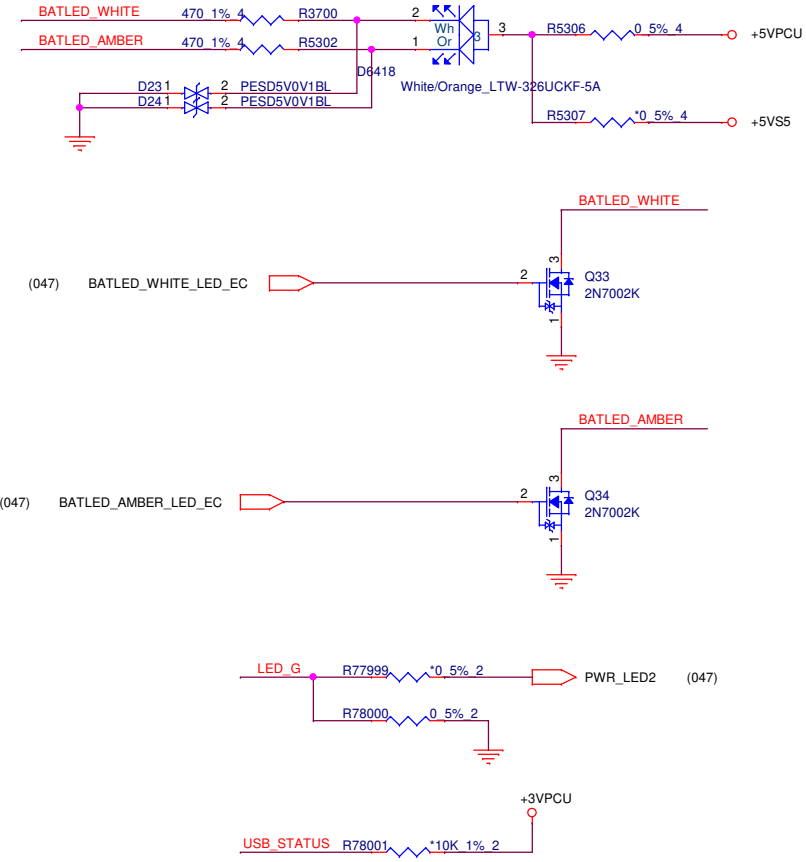




BU2	PROJECT : LS2B Quanta Computer Inc.	
Size	Document Number Touch Pad/Fingerprint	Rev 1A
Date: Friday, September 25, 2020	Sheet 52 of 84	

Daughter Board





BU2

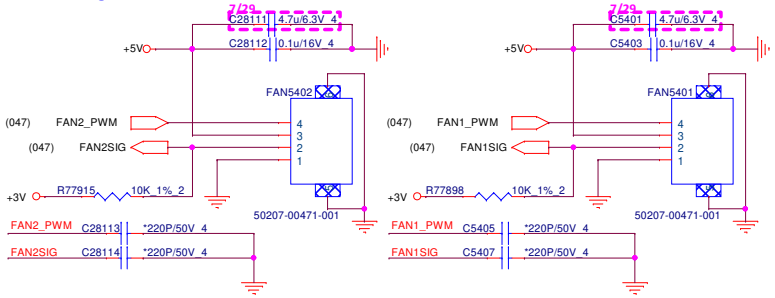
PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	Switch/DB/LED	1A

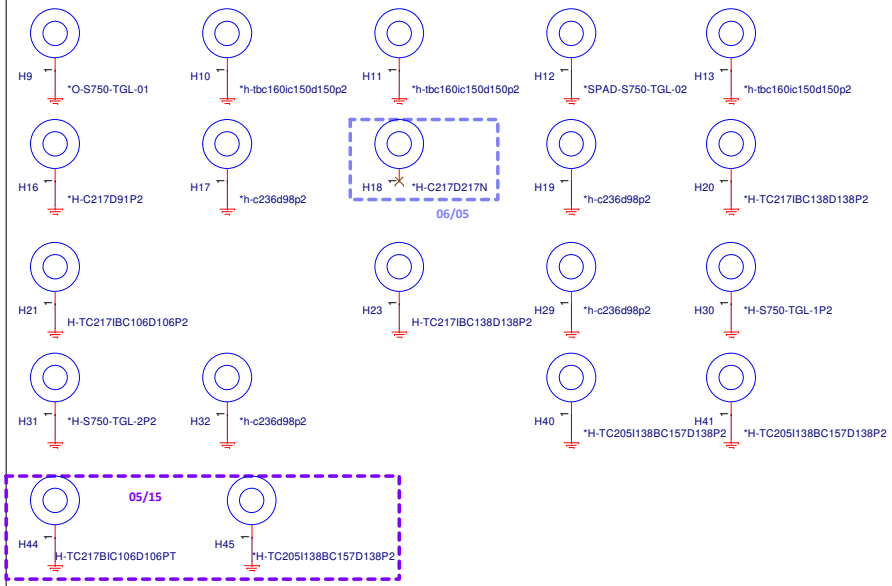
Date: Friday, September 25, 2020 Sheet 53 of 84

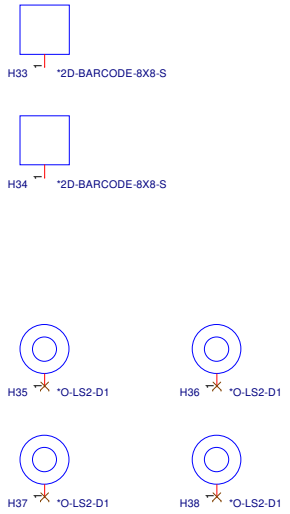
FAN/Thermal



8/4

Hole





Nuvoton	NCT7718W	SMBus Address	98h	AL007718001
Nuvoton	W83L771AWG-2	SMBus Address	9Ah	AL83L771K03
GMT	G781P8	SMBus Address	98h	AL000781012
GMT	G781-1P8	SMBus Address	9Ah	AL000781039

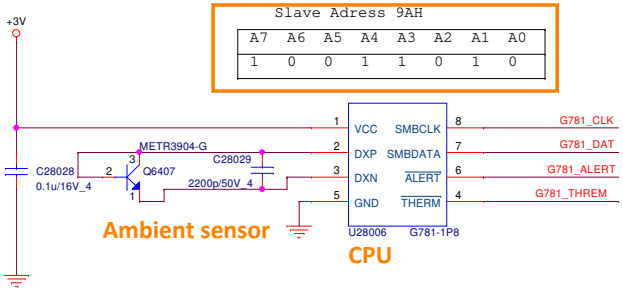
Thermal Sensor

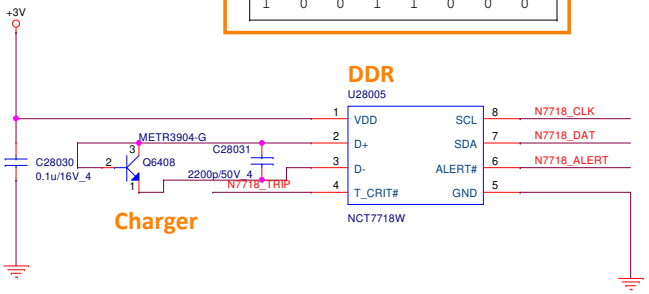
Slave Adress 9AH

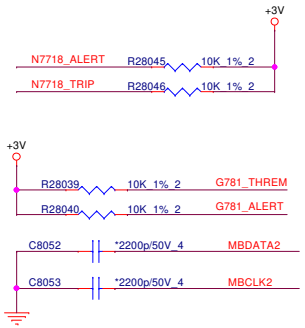
A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	1	0

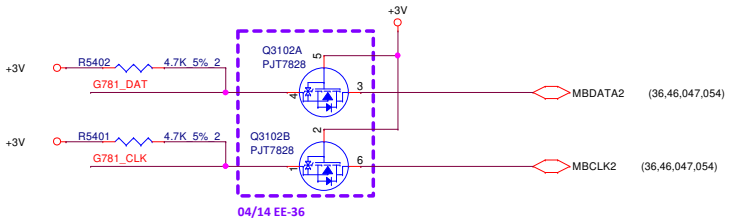
Slave Adress 98H

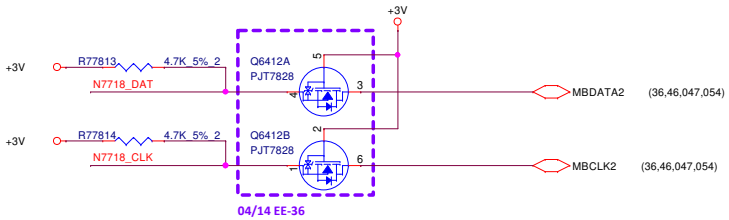
A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	0	0











BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal Sensor	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	Card Reader	1A

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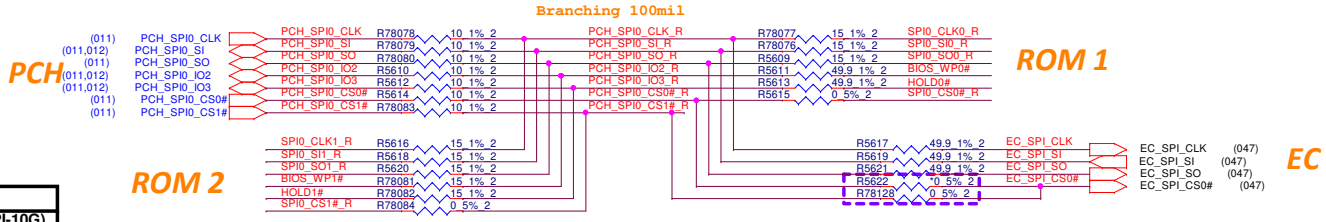
FLASH ROM

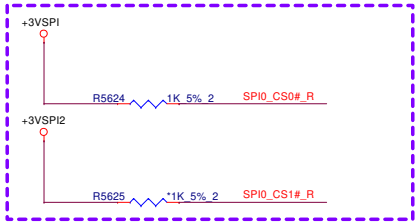


PCH SPI ROM

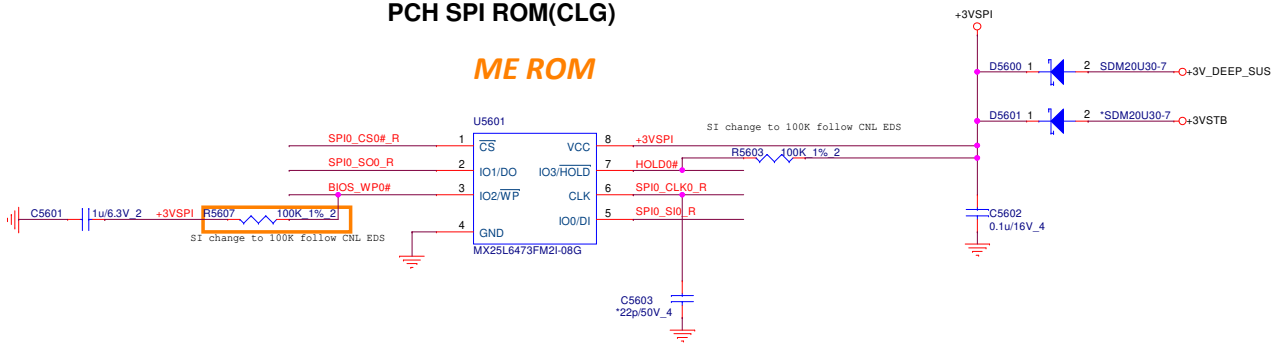
Vender	Size	P/N
MXIC	16MB	AKE3DZN0Z08(MX25L12872FM2I-10G)
Winbond	16MB	AKE3DF-KN01(W25Q128JVSIQ)
GGD	16MB	AKE3DZN0Q02(GD25B127DSIGR)
MXIC	8MB	AKE3EZ-0Z00(MX25L6473FM2I-08G)
Winbond	8MB	AKE3EZ-0N01(W25Q64JVSSIQ)
GGD	8MB	AKE2EZN0Q00(GD25B64CSIGR)
Socket		DG008000011

PCH SPI ROM(CLG)

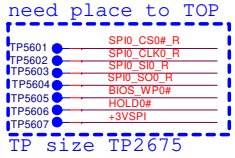
04/20 EE-38



ME ROM

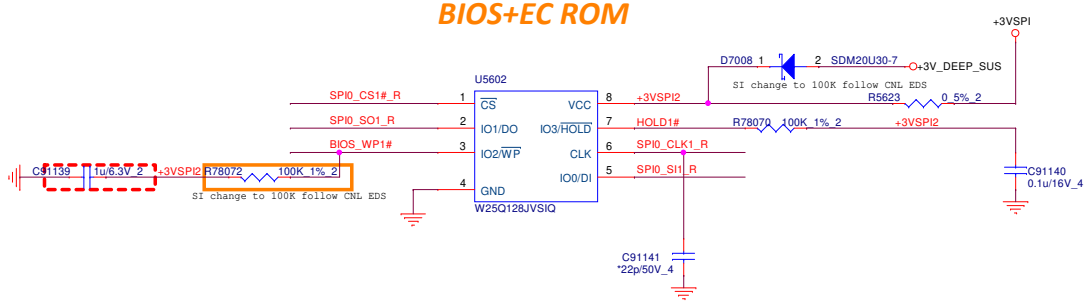


need place to TOP

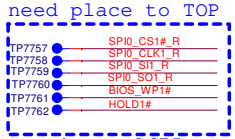


TP size TP2675

BIOS+EC ROM



need place to TOP



TP size TP2675

BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	FLASH ROM	1A

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PROJECT : LS2B

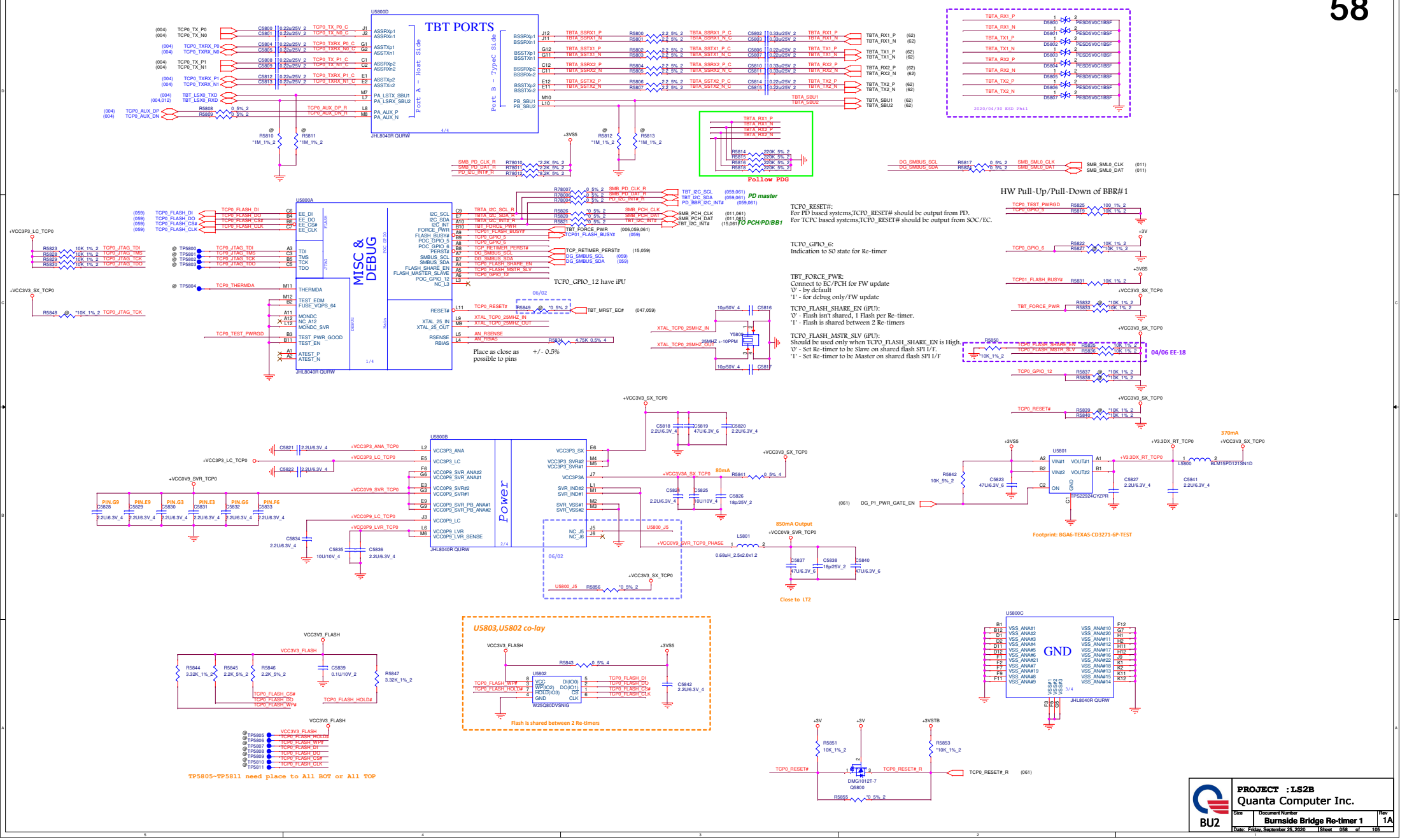
Quanta Computer Inc.

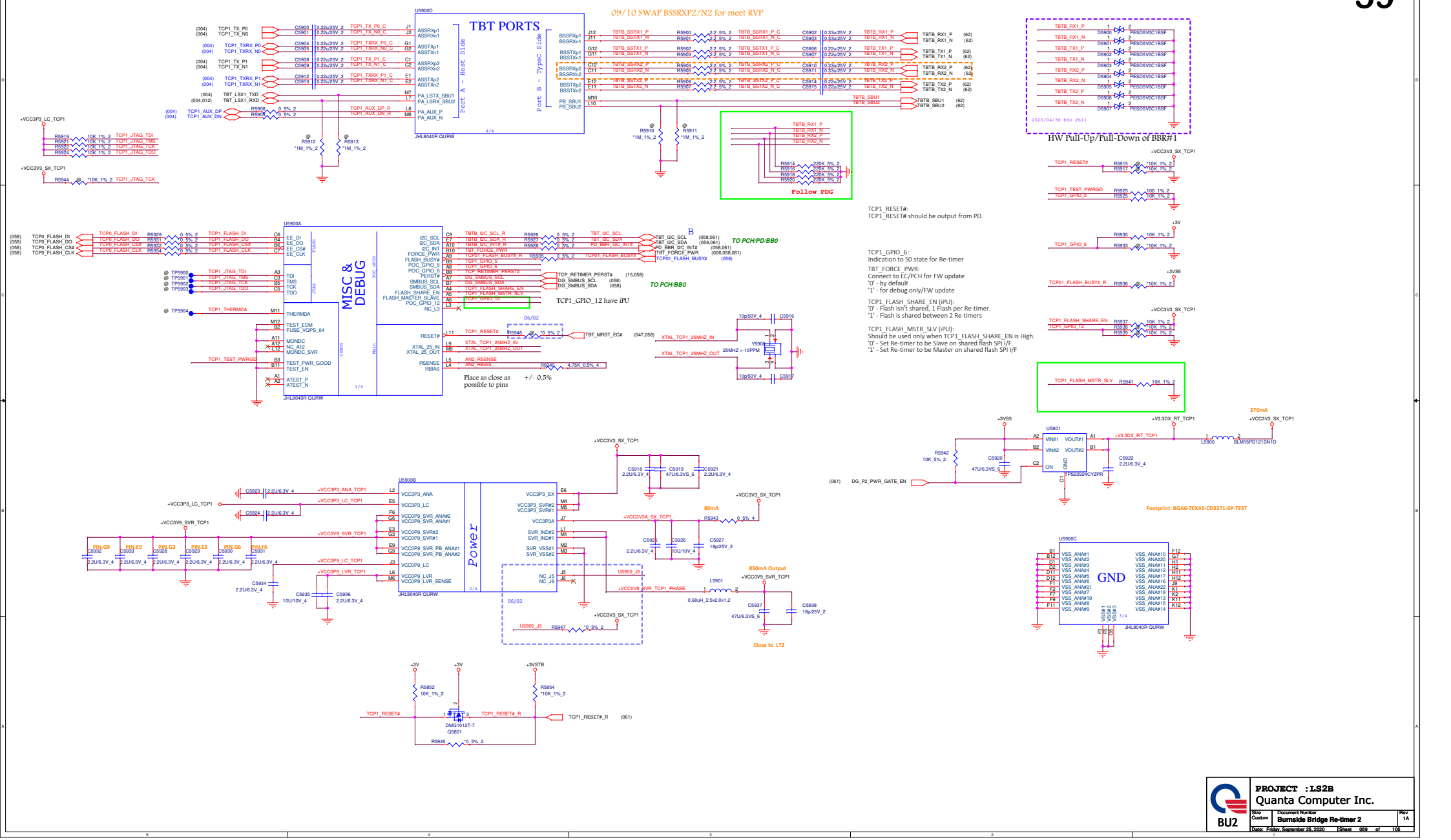
Size	Document Number: LS2	Rev
BU2		
Date:	Sheet of	

USB type A 1A

Friday, September 25, 2020 57 84

AJ0QURW0U01





PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Burnside Bridge Re-timer 2	1A

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	Thunderbolt & Type C	1A

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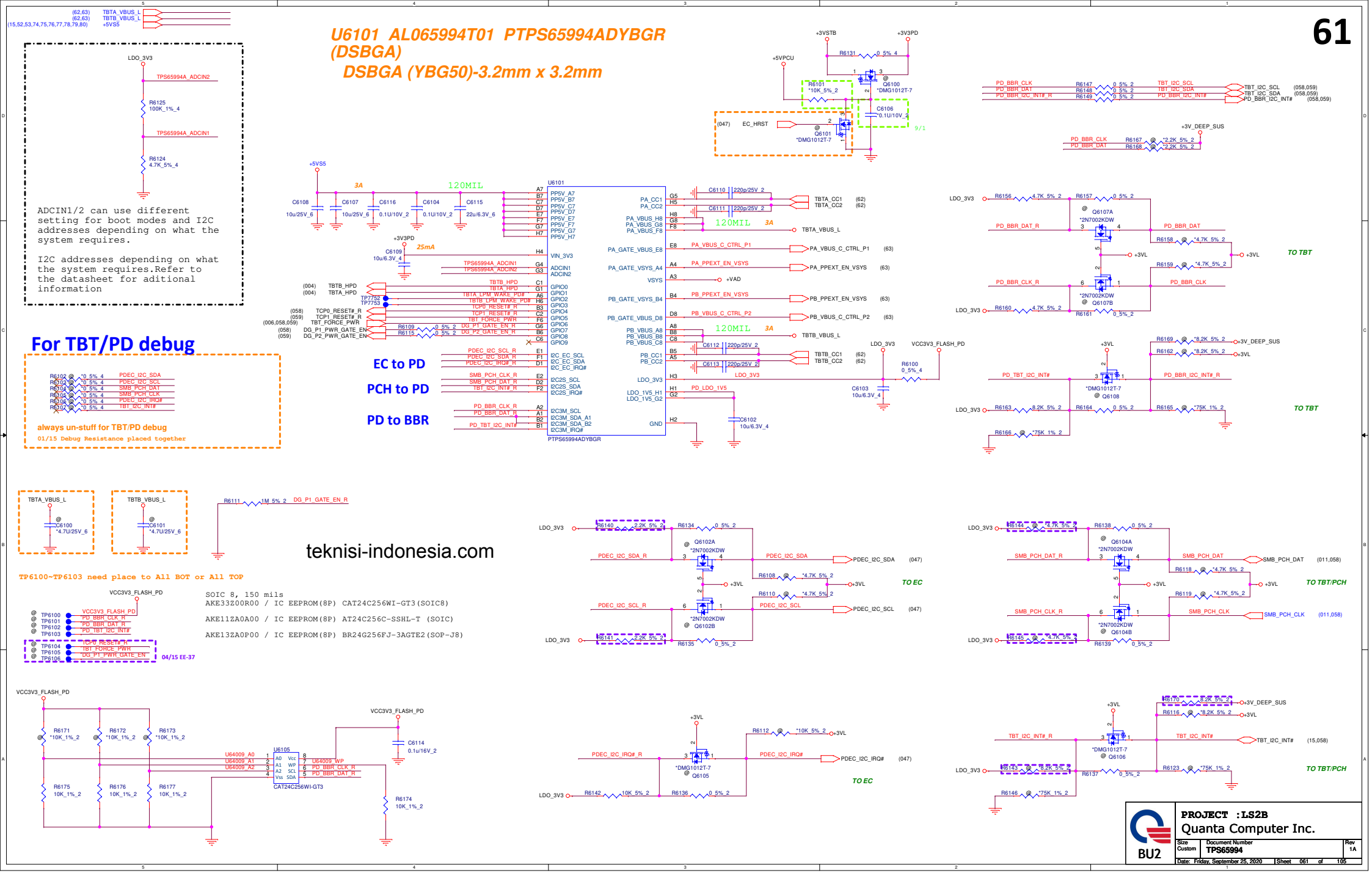
U6101 AL065994T01 PTPS65994ADYBGR (DSBGA)

DSBGA (YBG50)-3.2mm x 3.2mm



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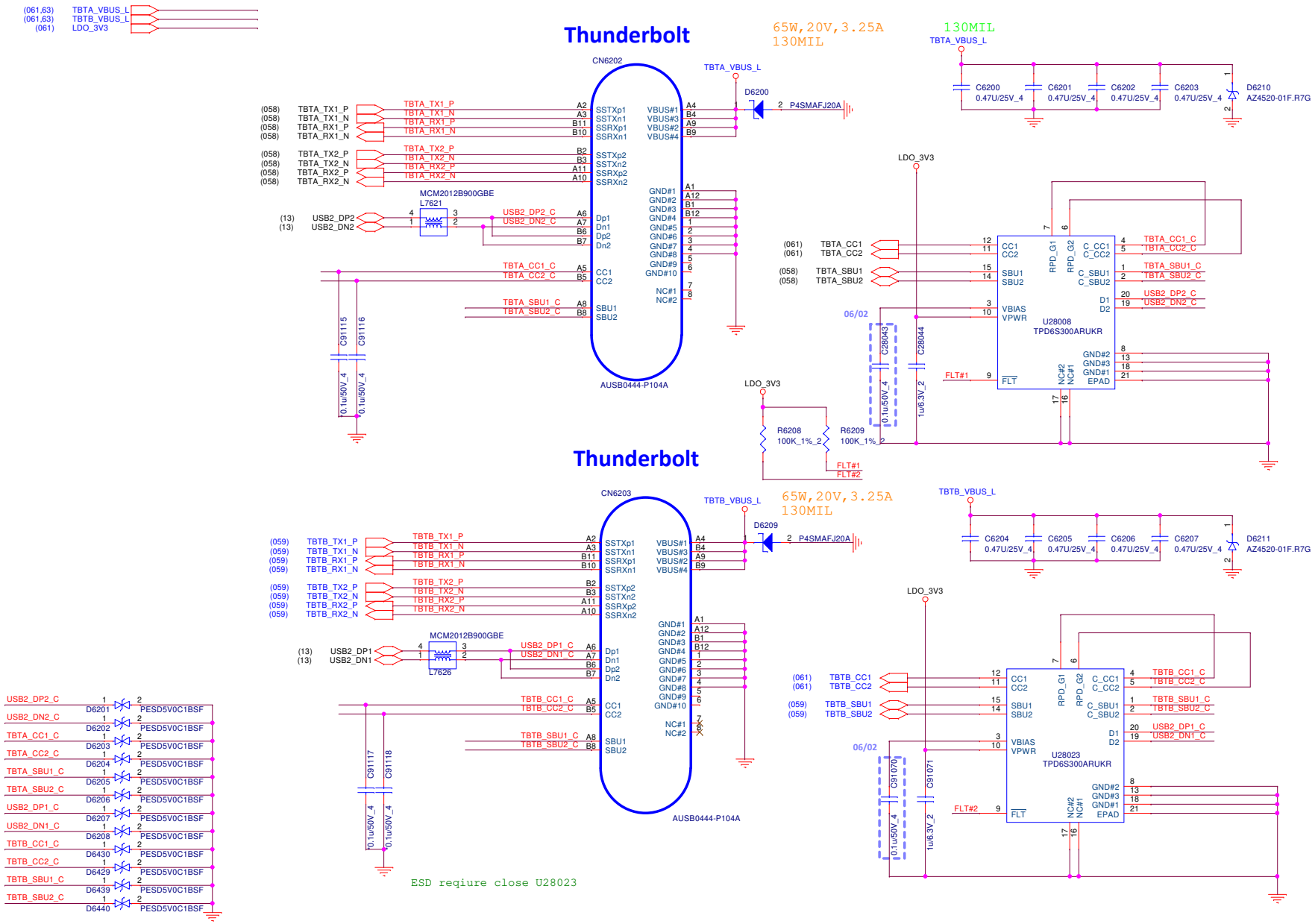
PROJECT :LS2B
Quanta Computer Inc.
BU2
Size Custom | Document Number TPS65994 | Rev 1A
Date: Friday, September 25, 2020 | Sheet 061 of 105


Thunderbolt
65W,20V,3.25A
130MIL
130MIL
CN6202
TBTA_VBUS_L
D6200
P4SMAFJ20A
C6200 0.47U/25V_4
C6201 0.47U/25V_4
C6202 0.47U/25V_4
C6203 0.47U/25V_4
D6210 AZ4520-01F.R7G
MCM2012B900GBE
L7621
AUSB0444-P104A
LDO_3V3
U28008
TPD6S300ARUKR
06/02
R6208 100K_1%_2
R6209 100K_1%_2
Thunderbolt
CN6203
TBTB_VBUS_L
D6209
C6204 0.47U/25V_4
C6205 0.47U/25V_4
C6206 0.47U/25V_4
C6207 0.47U/25V_4
D6211 AZ4520-01F.R7G
MCM2012B900GBE
L7626
U28023
TPD6S300ARUKR
ESD reqiure close U28023
USB and DP x 4 USB Type-C Connector Mapping (Up Side Down)
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
GND DP ML0+ DP ML0- VBUS CC1 USBD- DP AUX- VBUS DP ML3- DP ML3+ GND
GND DP ML2+ DP ML2- VBUS DP AUX+ USBD+ CC2 VBUS DP ML1- DP ML1+ GND
B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1
PROJECT :LS2B
Quanta Computer Inc.
BU2
Size
Document Number
USB TYPE-C_Port A,B
Rev
1A
Date: Friday, September 25, 2020
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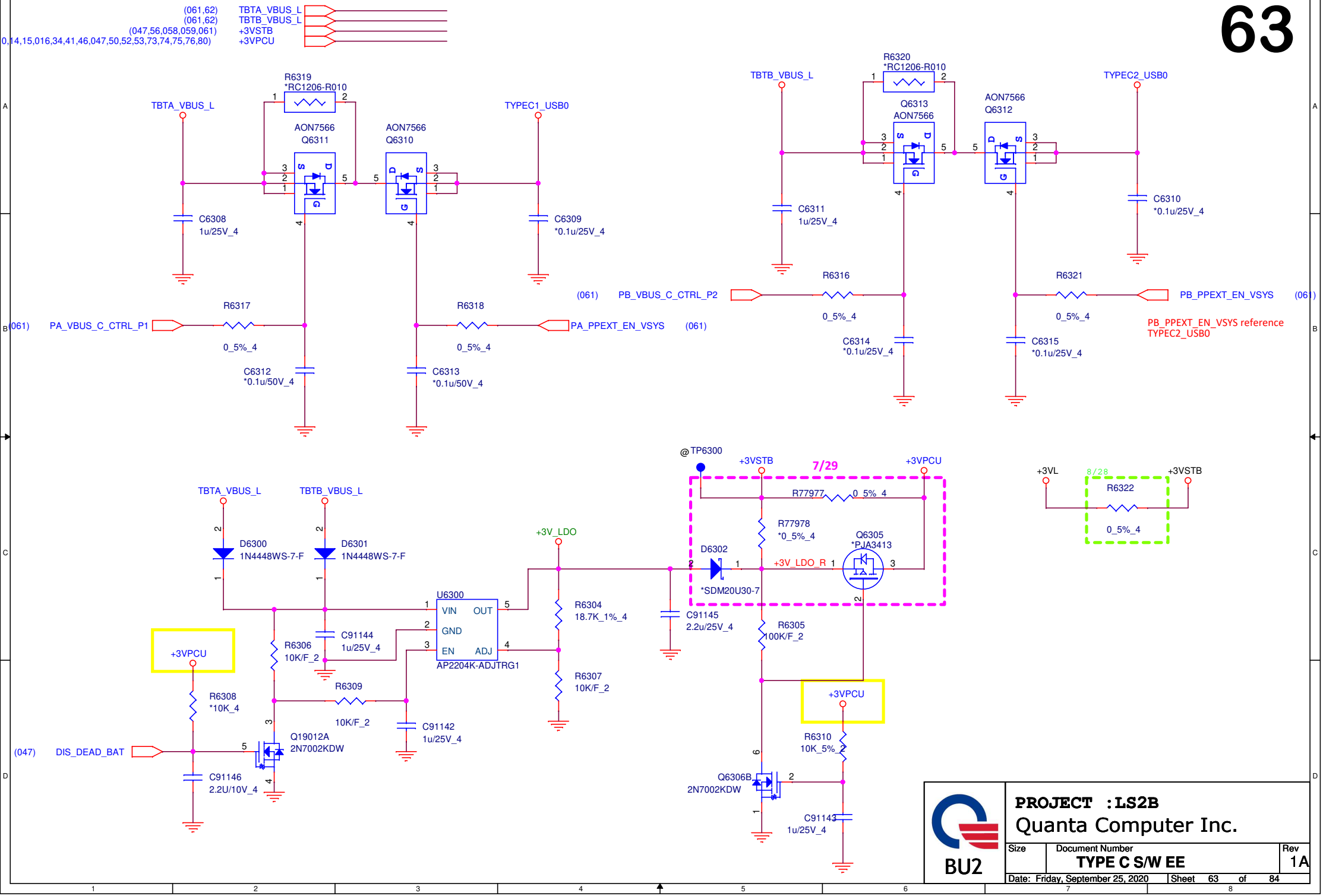

BU2

PROJECT :LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	TYPE C S/W EE	1A

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TYPE-C Load Switch

Quanta confidential

BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	NC	1A

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Reserve

Quanta confidential

BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	USB type C /NC	1A

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Reserve

Quanta Confidential

BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	dGPU /NC	1A

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Reserve

Quanta Confidential

Reserve

Quanta confidential

Reserve

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BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
Custom	dGPU /NC for ERD check	1A

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Reserve

BU2	PROJECT : LS2B Quanta Computer Inc.	
Size Custom	Document Number dGPU /NC for ERD check	Rev 1A
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Reserve

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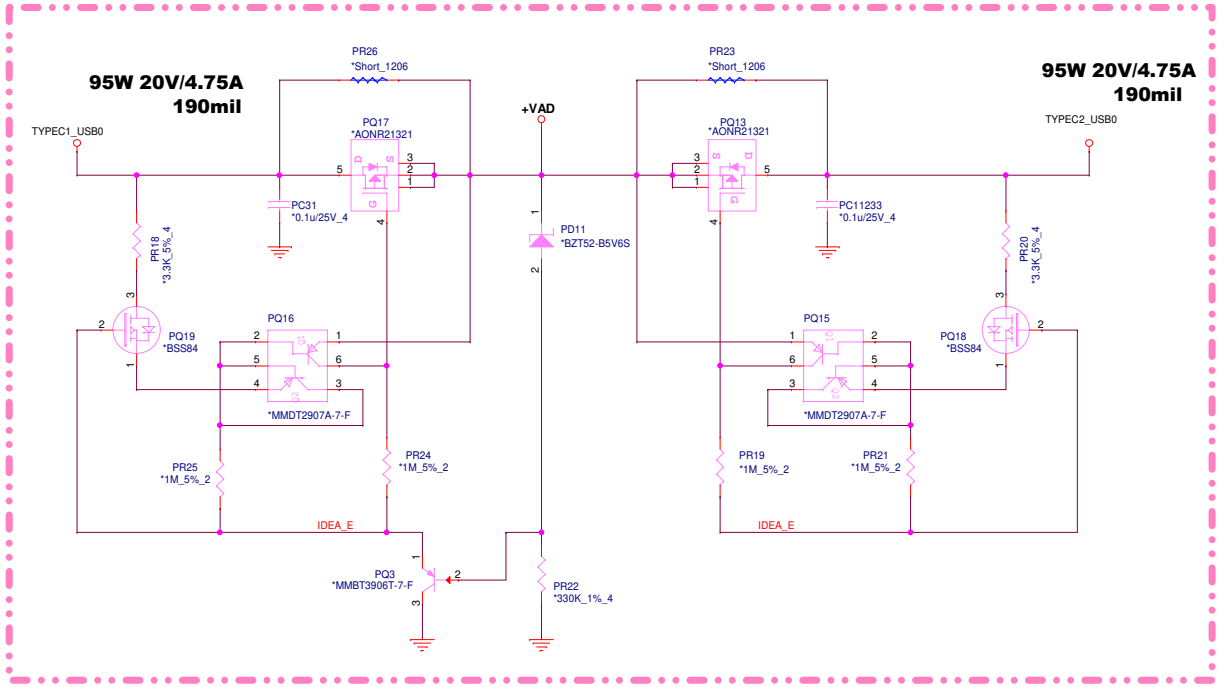
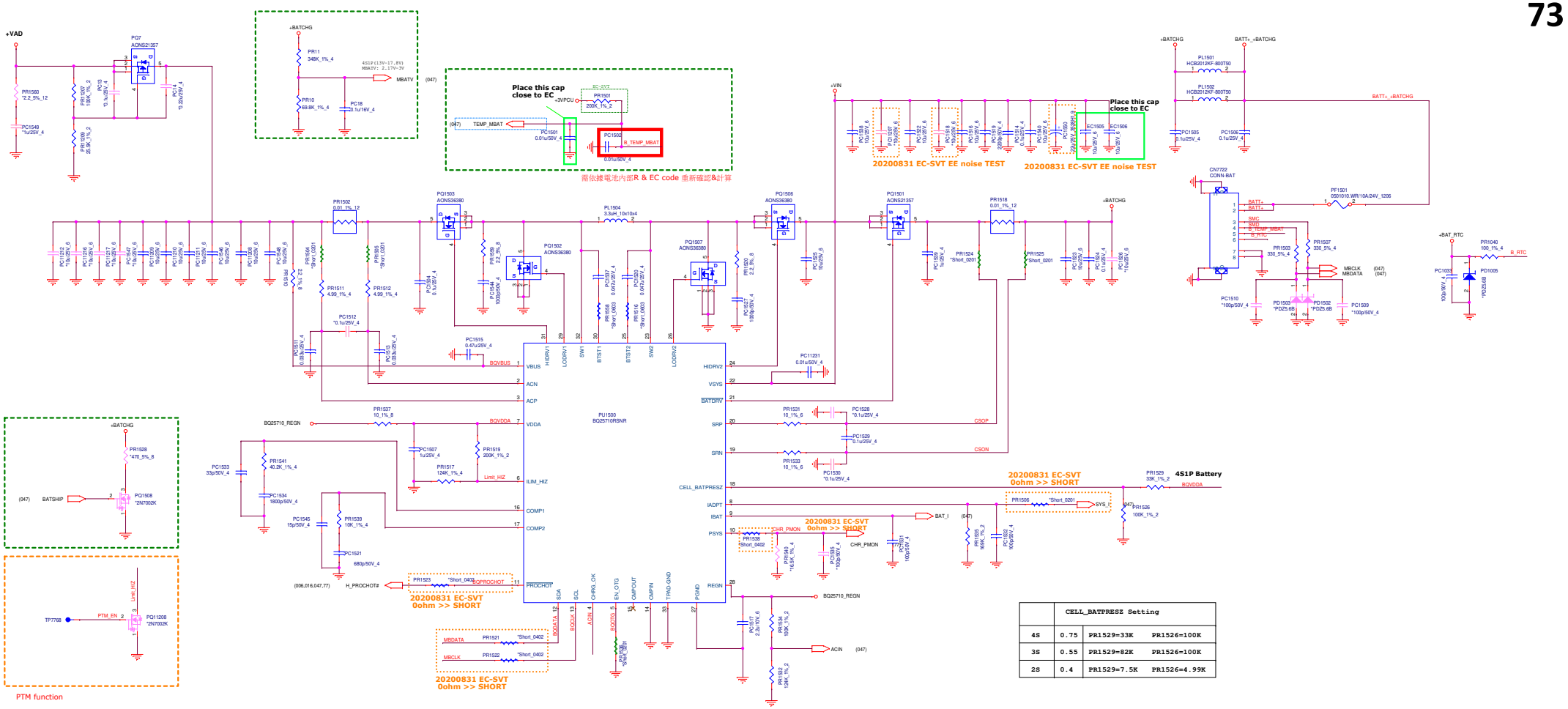
For TypeC PORT1

For TypeC PORT2

20200803 EC-SIT-R TEST

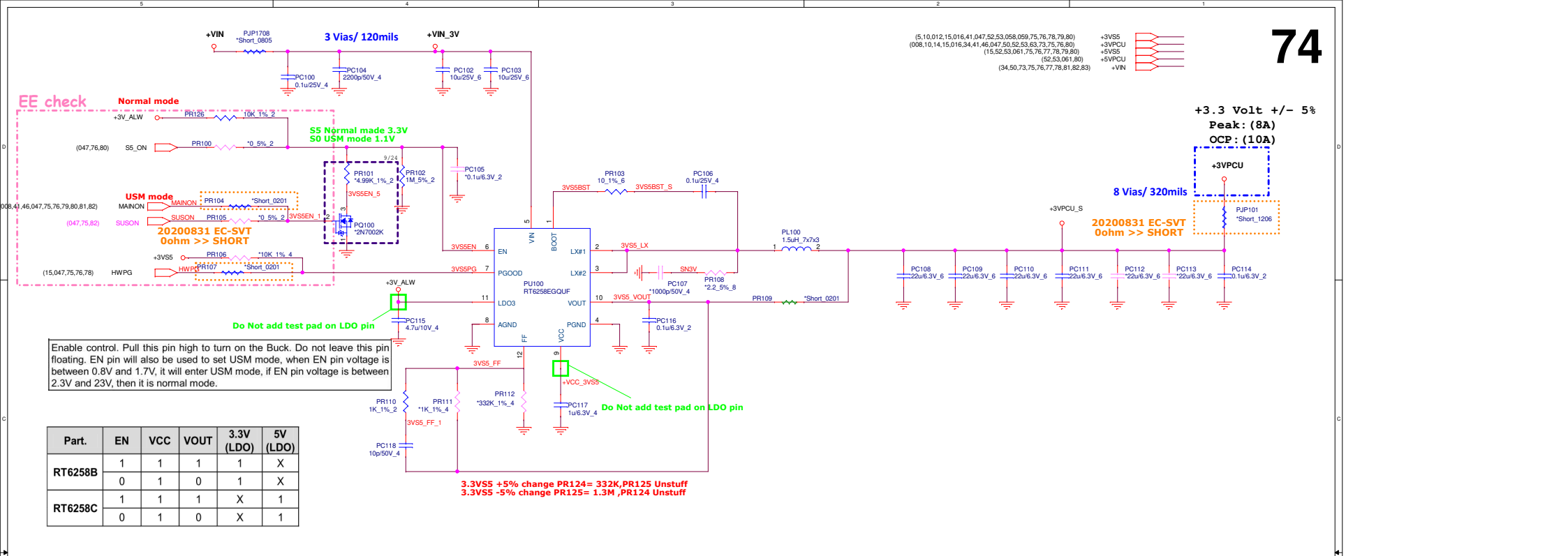


BU2	PROJECT : LS2B Quanta Computer Inc.	
Size Custom	Document Number TYPEC load switch MOSFET	Rev 1A
Date Friday, September 25, 2020	Sheet 72 of 84	



	CELL_BATPRESZ Setting		
4S	0.75	PR1529=33K	PR1526=100K
3S	0.55	PR1529=82K	PR1526=100K
2S	0.4	PR1529=7.5K	PR1526=4.99K

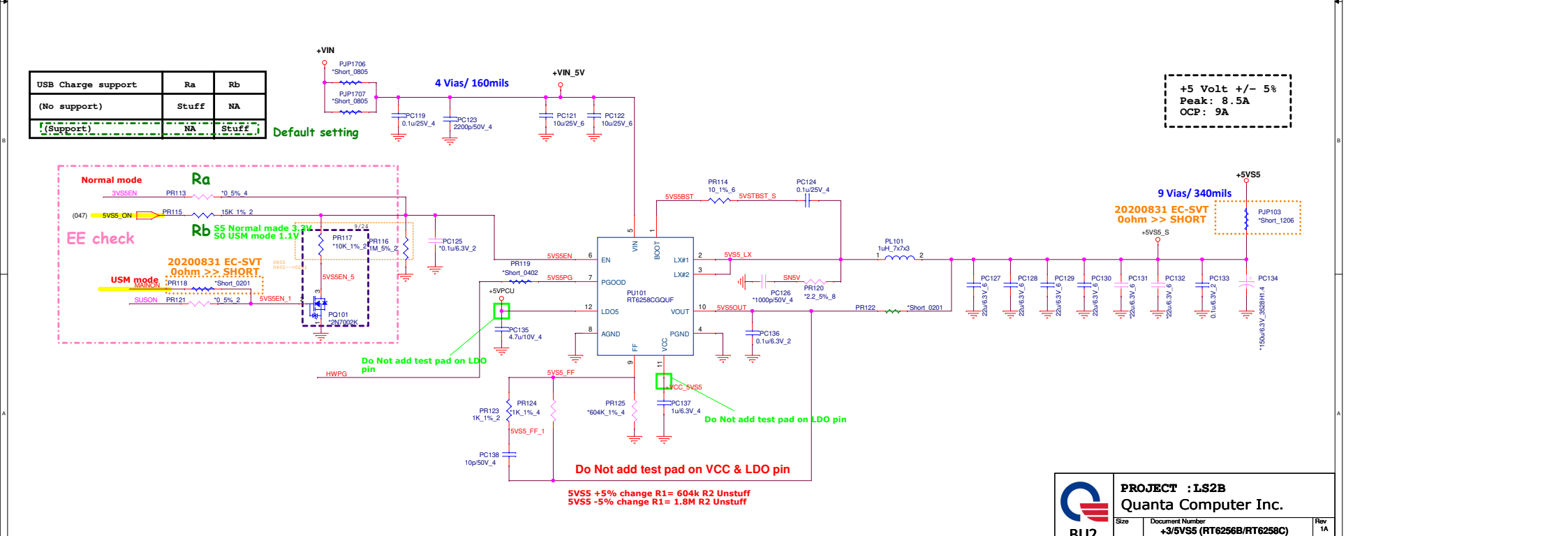
PROJECT : LS2B
Quanta Computer Inc.
BU2
Size | Document Number: Charger (BQ25710RSNR) | Rev 1A
Date: Friday, September 25, 2020 | Sheet 73 of 84



Enable control. Pull this pin high to turn on the Buck. Do not leave this pin floating. EN pin will also be used to set USM mode, when EN pin voltage is between 0.8V and 1.7V, it will enter USM mode, if EN pin voltage is between 2.3V and 23V, then it is normal mode.

Part.	EN	VCC	VOUT	3.3V (LDO)	5V (LDO)
RT6258B	1	1	1	1	X
	0	1	0	1	X
RT6258C	1	1	1	X	1
	0	1	0	X	1

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff



BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	+3/5VS5 (RT6256B/RT6258C)	1A

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(5,10,012,15,016,41,047,52,53,058,059,74,76,78,79,80) +3VS5
(34,50,73,74,76,77,78,81,82,83) +VIN

EE check

+3VS5 PR221 *100K_1%_4
(15,047,74,76,78) HWPG PR222 *Short_0402

(047,74,75,82) SUSON PR223 *Short_0402 PC201 *1u/10V_4
20200831 EC-SVT
0ohm >> SHORT
(5) DDR_VTT_PG_CTRL_R PR224 *0_5%_4
(008,41,46,047,74,76,79,80,81,82) MAINON PR226 *Short_0402 PC202 *1u/6.3V_4

Table 2. S3 and S5 truth table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

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PR225 430K_1%_4
OCP = current limit + Iripple/2
= (430K*5uA/10/15.9mohm) + (2.8/2)=15A

PR228 620K_1%_4 1P35V_TON
Place these CAPs close to FETs
VIN_8231 PR229 *Short_0805 +VIN
PC203 2200p/50V_4 PC204 0.1u/25V_4 PC205 10u/25V_6 PC206 10u/25V_6 PC207 0.1u/25V_4

+1.2VSUS+/-5%
Imax= 13.5A
OCP minimum: 15A

+0.6V_DDR_VTT_R PR230 *Short_0603 +0.6V_DDR_VTT
20200831 EC-SVT
0ohm >> SHORT
PC209 10u/6.3V_4
DDR_VTTREF PR232 100_5%_4 1P35V_VTTREF
PC210 0.1u/16V_4 PC211 0.033u/50V_6
+1.2VSUS_R PC216 10u/6.3V_4

PU200
RT8231BGQW
VTT, VTTSNS, VTTGND, VTTREF, VLDOIN, S3, S5, PGOOD, CS, TON, UGATE, BOOT1, PHASE, LGATE, VDD, LPMB, VID, PGND, FB, VDDQ, PAD

1P35V_UGATE PR231 1_1%_6 PC208 0.1u/25V_4 DDR1
1P35V_BOOT
1P35V_PHASE
1P35V_LGATE
1P35V_VDD PR233 *Short_0603 +5VS5 PC212 1u/6.3V_4
20200831 EC-SVT
0ohm >> SHORT

PQ210 AONR32320C
PQ211 AONR36326C
Rds(on)=13-15.9m ohm
AONR36326 Rdson = 15.9m Ohms

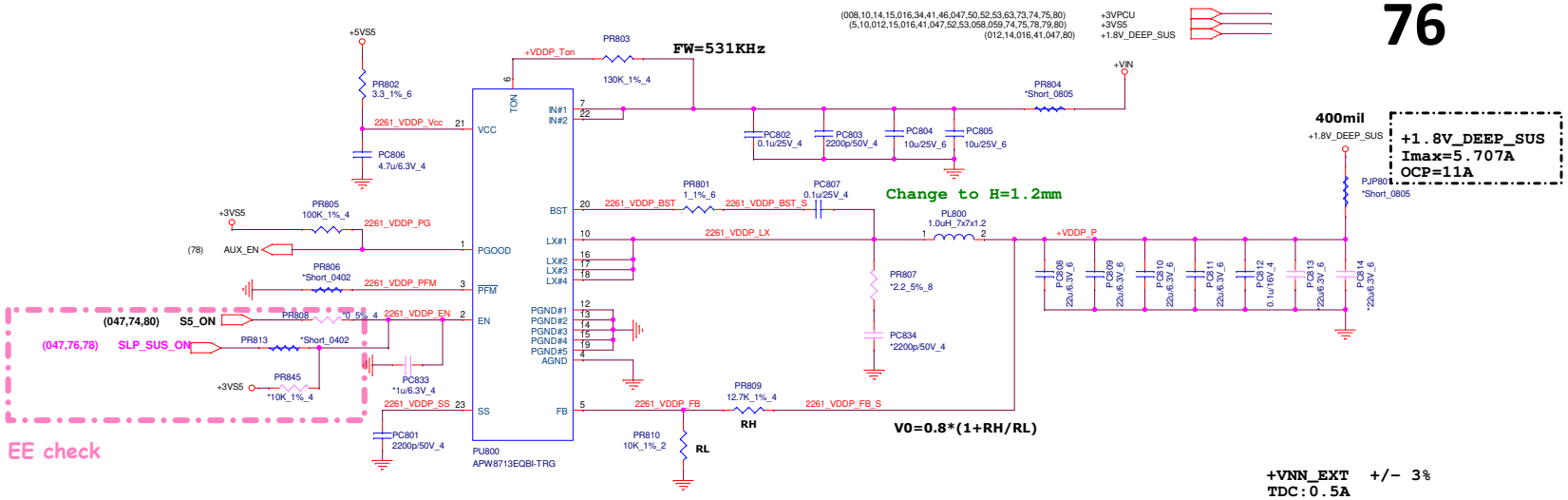
PL200 1uH_7x7x3 +1.2VSUS_R
PR234 *2.2_5%_8 DDR2 PC217 *2200p/50V_4
PC213 330u/2.5V_3528H1.9 PC214 10u/6.3V_4 PC215 0.1u/16V_4 PC221 22u/6.3V_6 PC222 22u/6.3V_6 PC223 22u/6.3V_6 PC224 22u/6.3V_6 PC225 22u/6.3V_6 PC226 22u/6.3V_6
PJP201 *Short_1206 +1.2VSUS

1P35V_LPMB 1P35V_VID 1P35V_FB 1P35V_VDDQ
*Short_0402 PR235 *Short_0402 PR236 +5VS5
20200831 EC-SVT
0ohm >> SHORT
R1 PR237 7.68K_1%_4 PR238 *Short_0402
PR239 10K_1%_4 R2
Vout = 0.675 * [1+(R1/R2)]

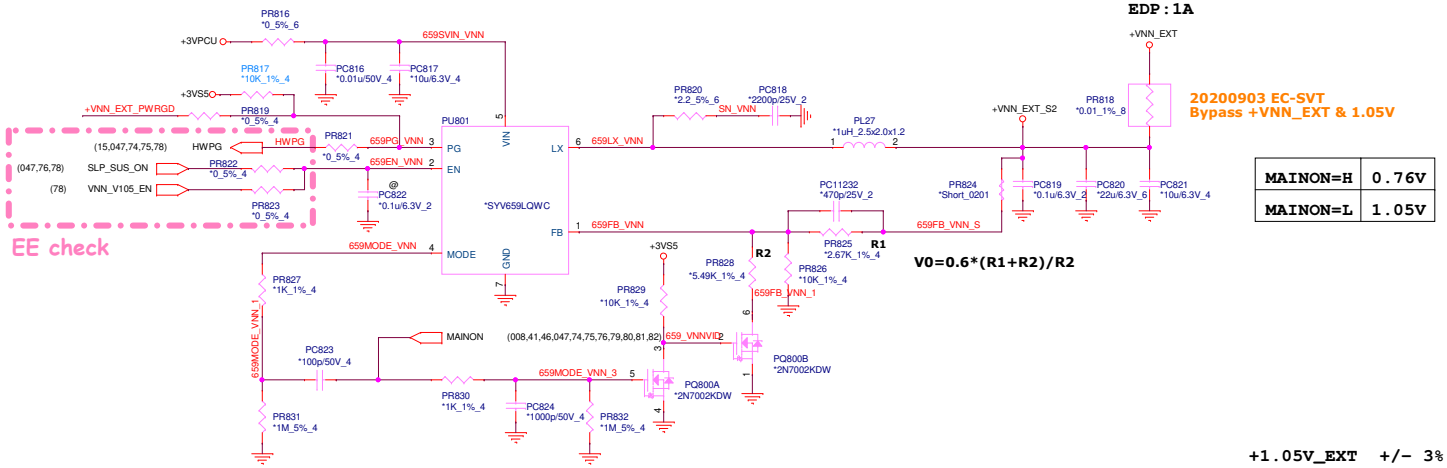
+5VS5 PR240 *Short_0402
+3VS5 PR241 10K_5%_4
PU201
G9661MF11U
VPP PGOOD VEN VO VIN GND1 GND2 ADJ NC
PG_+2.5V_S3
+2.5V_VIN PC218 1u/6.3V_4 PR242 *Short_0402 (047,74,75,82) SUSON
PR244 *Short_0805 +3VPCU
PC219 10u/6.3V_4 PC220 0.1u/16V_4
R1 PR245 21.5K_1%_4 +2.5V_ADJ R2 PR246 10K_1%_4
Vout = 0.8[1+(R1/R2)]
= 2.52
+2.5V_SUS_P PR243 *Short_0805 +2.5V_SUS
PC253 0.1u/16V_4 PC254 10u/6.3V_4 PC255 10u/6.3V_4

+2.5V
TDC:0.76A
100mil
EDP:1A

BU2
PROJECT :LS2B
Quanta Computer Inc.
Size | Document Number: DDR4 (RT8231BGQW) | Rev 1A
Date: Friday, September 25, 2020 | Sheet 75 of 84

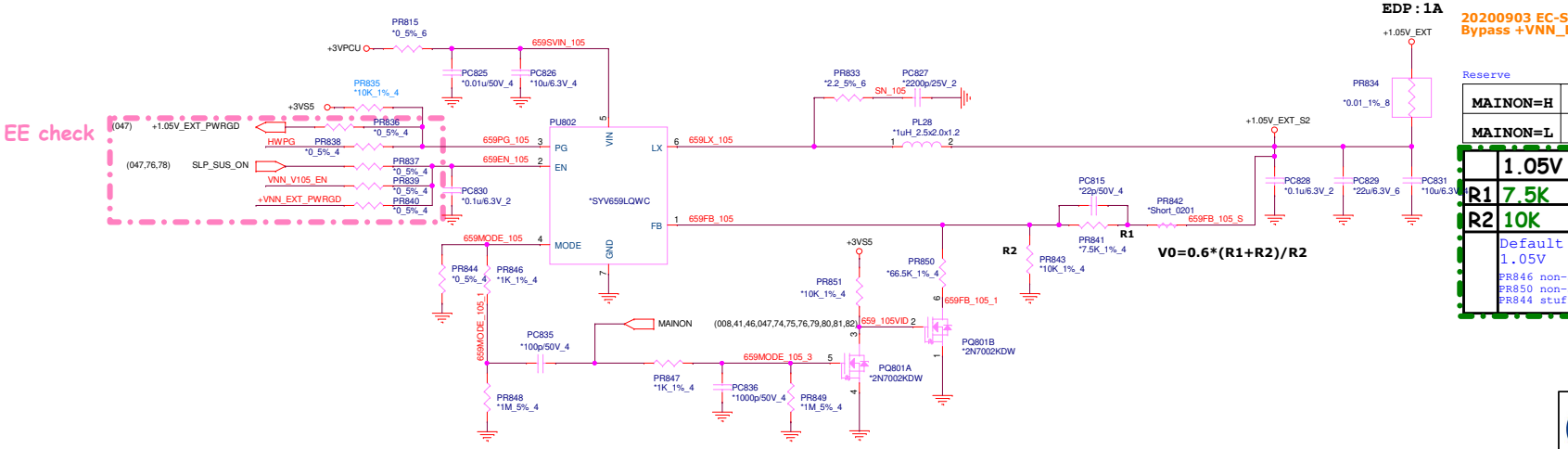


+VNN_EXT +/- 3%
TDC:0.5A
EDP:1A



MAINON=H	0.76V
MAINON=L	1.05V

+1.05V_EXT +/- 3%
TDC:0.5A
EDP:1A

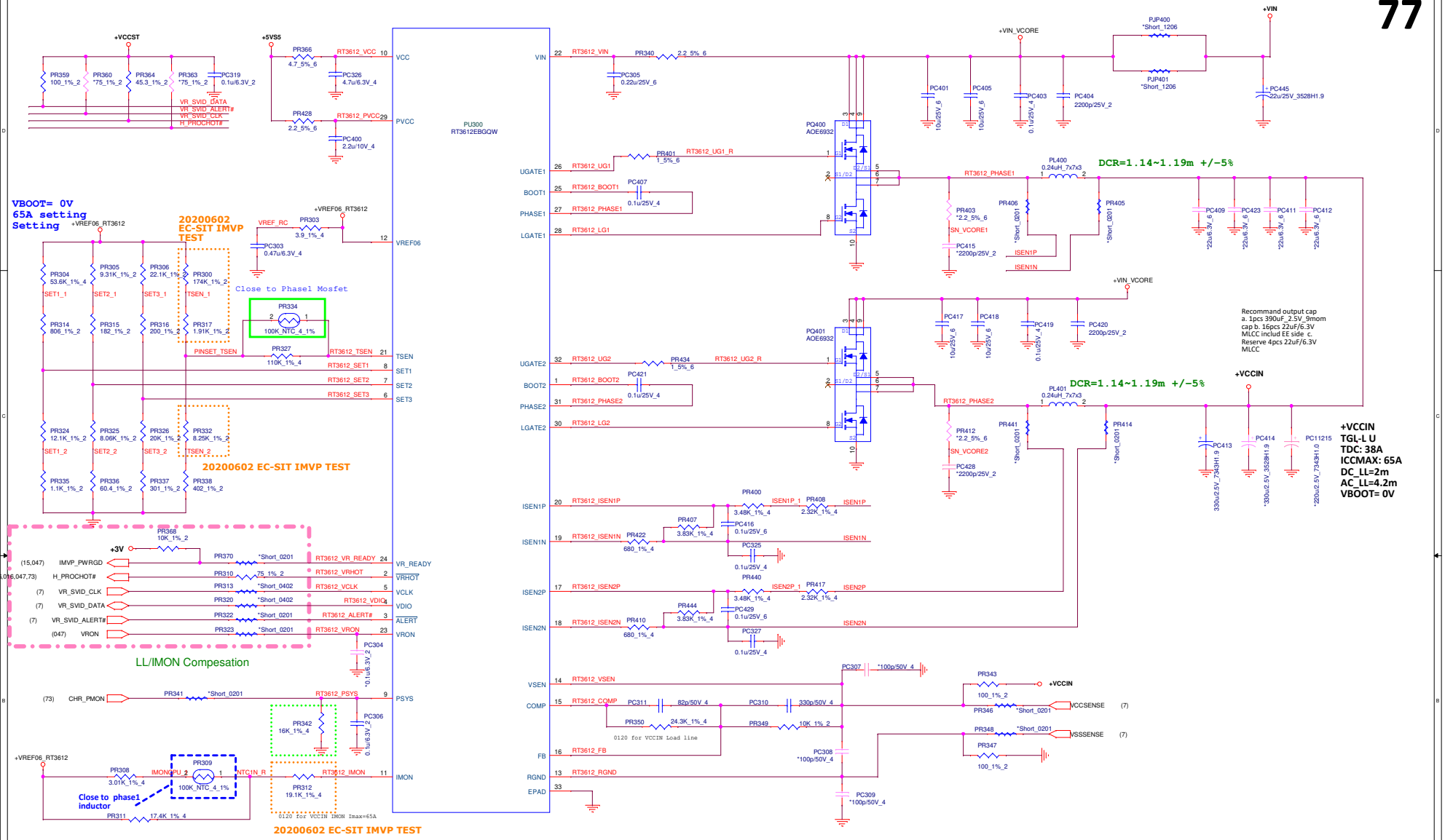


Reserve

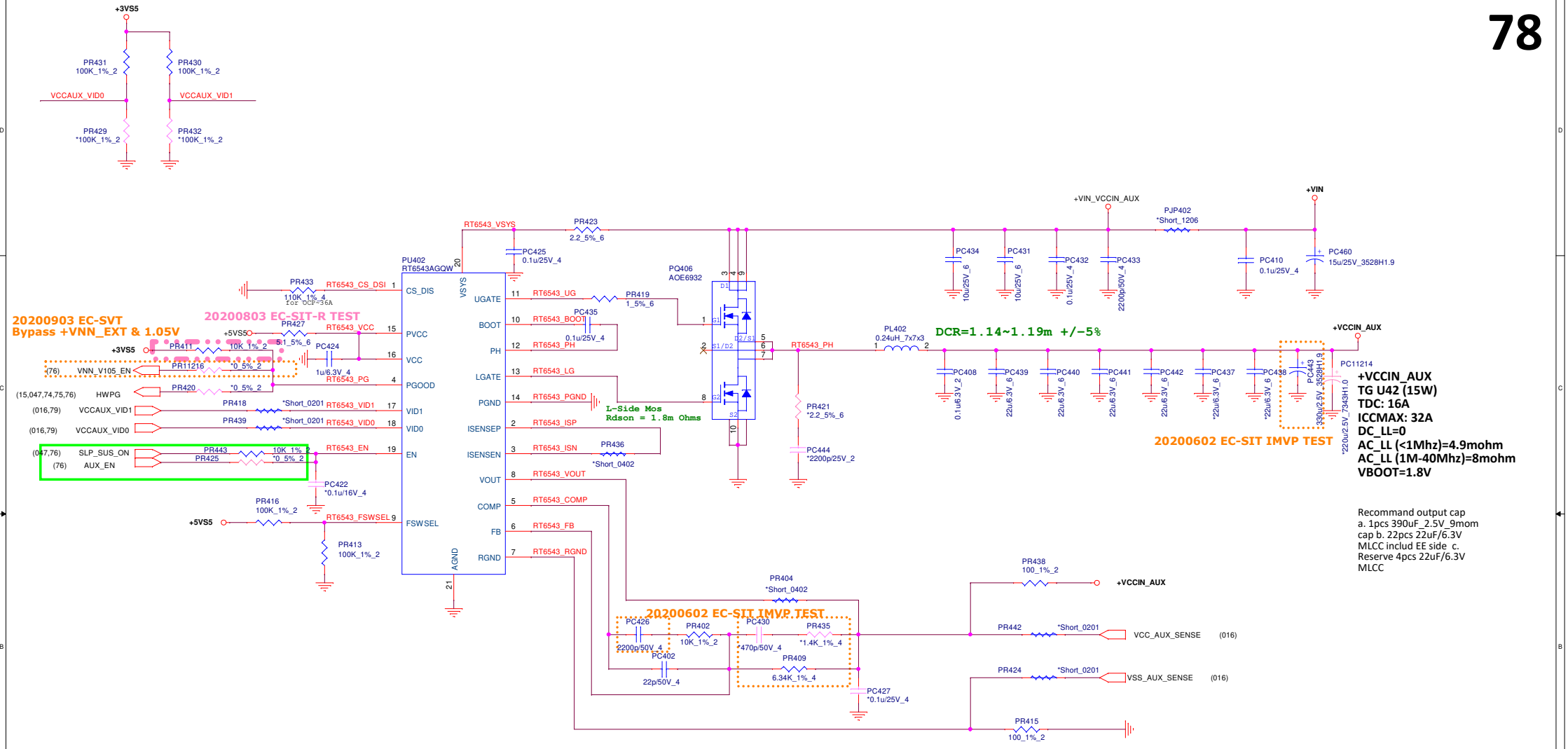
MAINON=H	0.96V
MAINON=L	1.05V

	1.05V	0.96V/1.05V
R1	7.5K	10K
R2	10K	16.5K
	Default 1.05V PR846 non-stuff PR850 non-stuff PR844 stuff	Switch H→0.95V L→1.05V PR846 stuff PR850 stuff PR844 non-stuff

PROJECT :LS2B
Quanta Computer Inc.
BU2
Size | Document Number: +1.8V_DEEP_SUS(RT8968) | Rev 1A
Date: Friday, September 25, 2020 | Sheet 76 of 84



BU2	PROJECT :LS2B Quanta Computer Inc.	
Size Custom	Document Number CPU VR IC (RT3612EBGQW-03)	Rev 1A
Date: Friday, September 25, 2020	Sheet 77 of 84	



BU2	PROJECT : LS2B Quanta Computer Inc.	
Size Custom	Document Number VCCIN_AUX IC (MP2941)	Rev 1A
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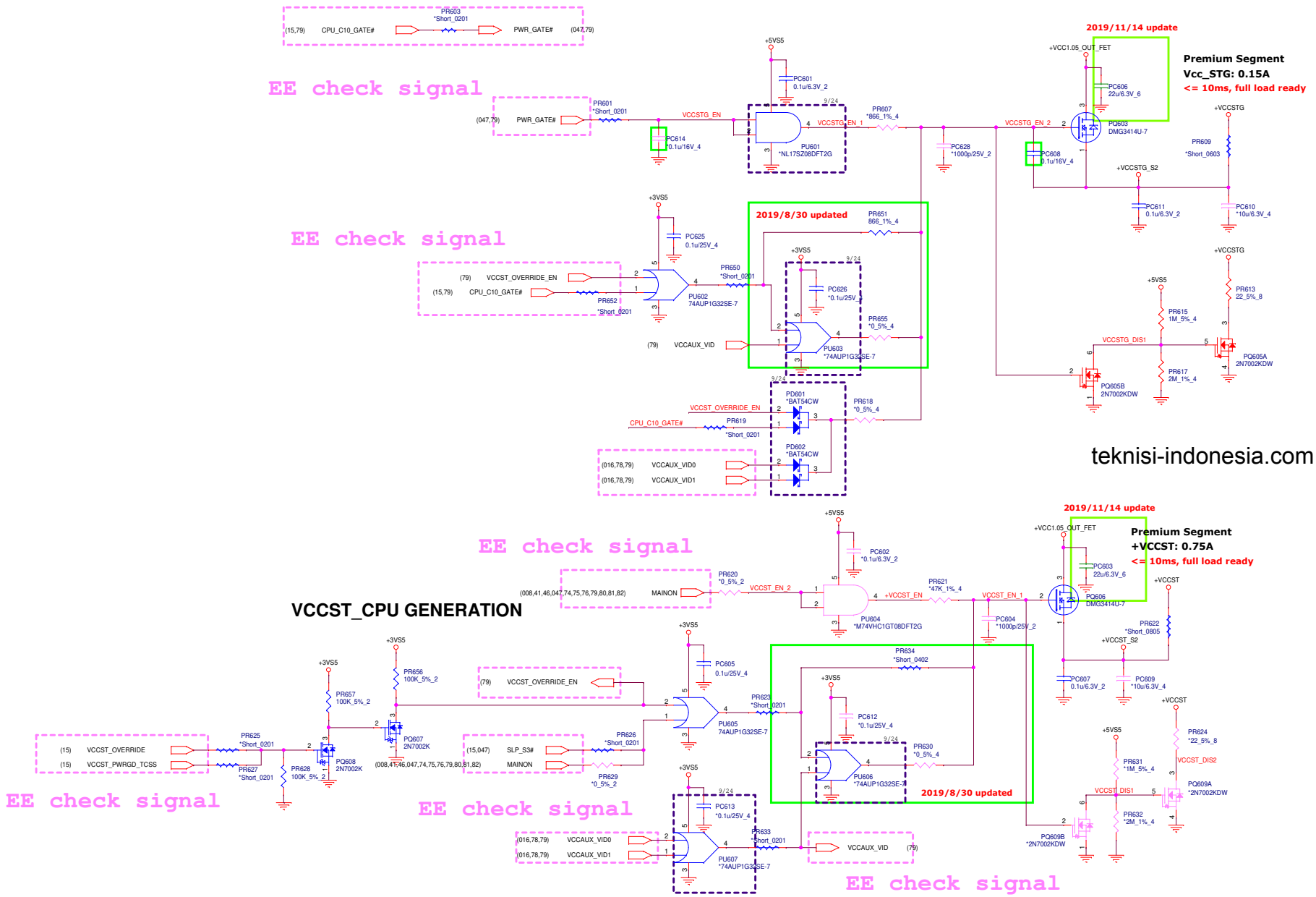
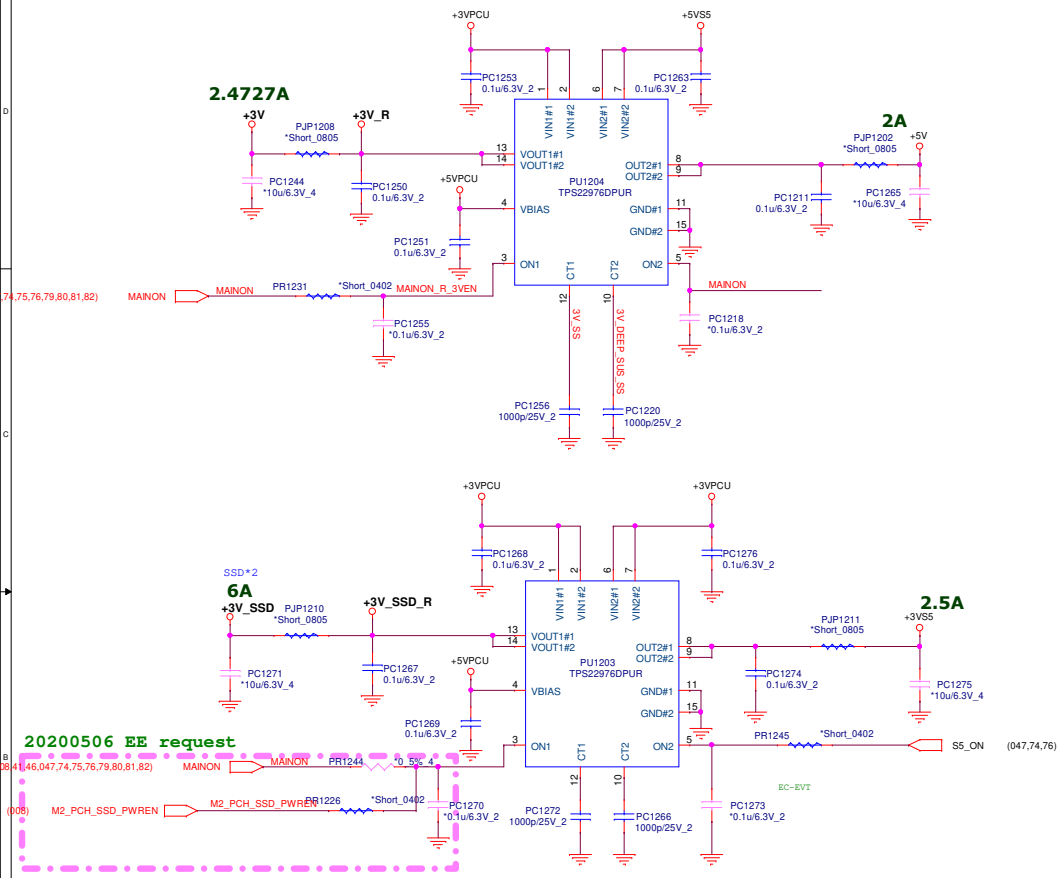
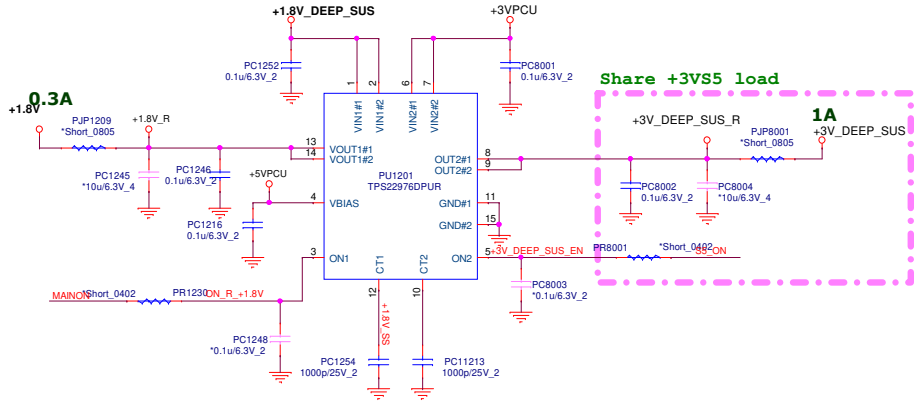


BU2	PROJECT : LS2B Quanta Computer Inc.	
Size C	Document Number +1.0V/+VCCSTPLL	Rev 1A
Date: Friday, September 25, 2020	Sheet 79 of 84	





BU2	PROJECT : LS2B Quanta Computer Inc.	
	Size / Document Number: Load switch IC (TPS22976)	Rev 1A
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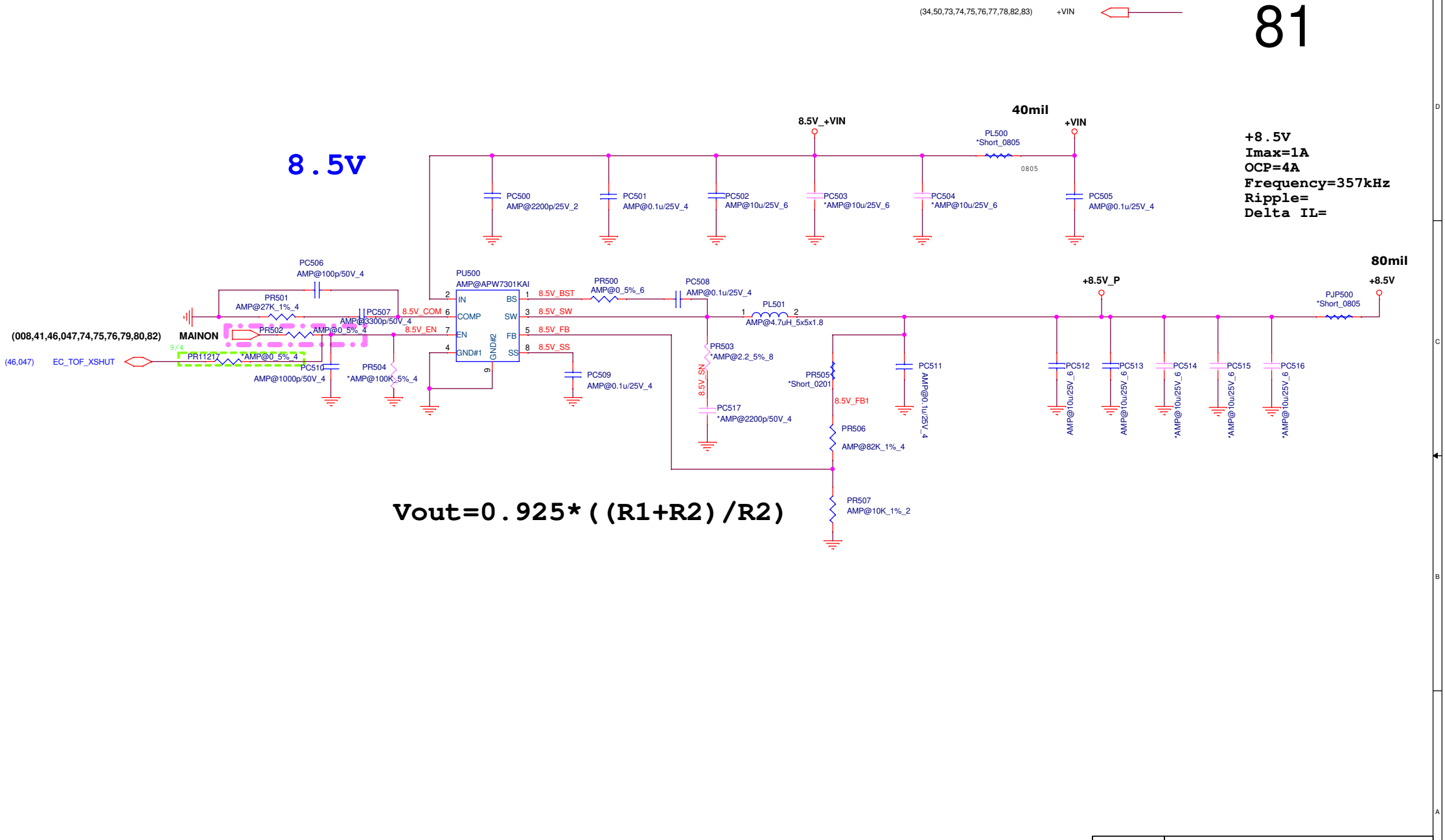

BU2	PROJECT :LS2B Quanta Computer Inc.	
Size	Document Number BU2	Rev 1A
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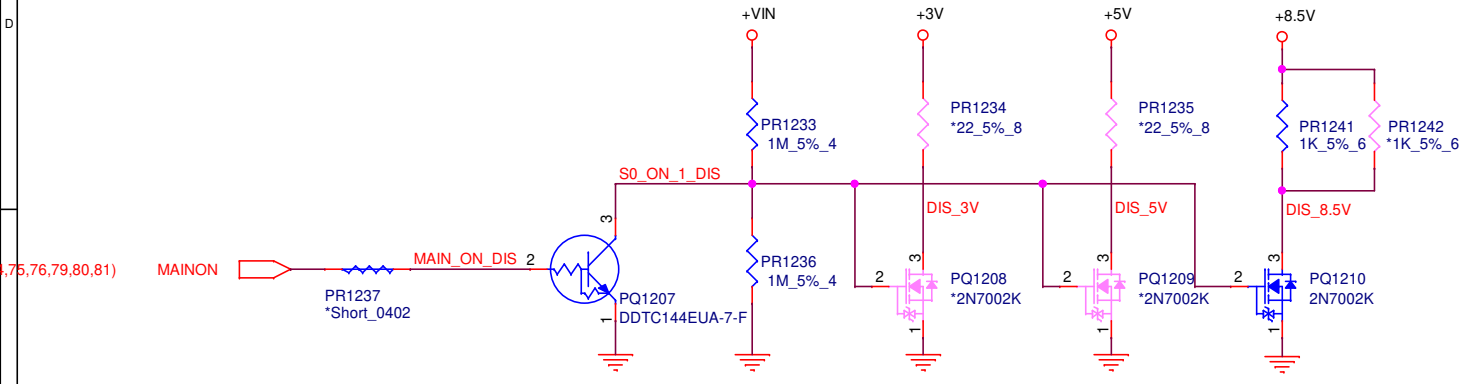
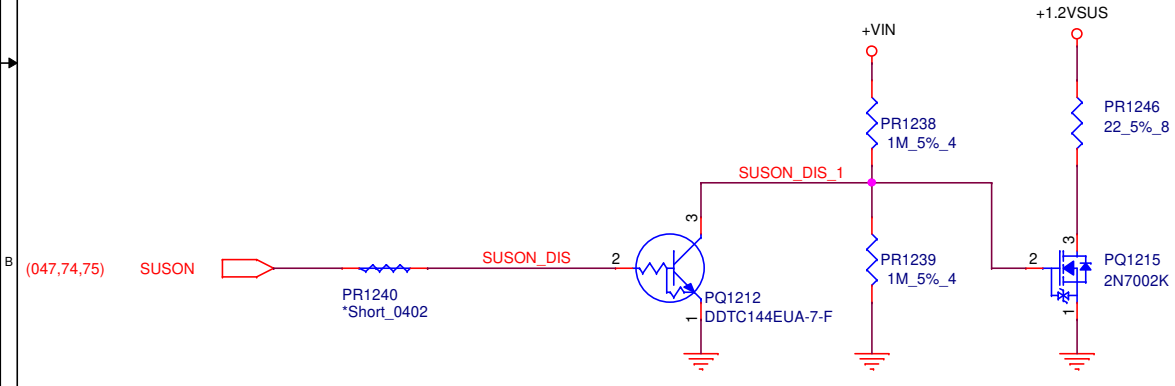
Power rail discharge



0120 add +8.5V discharge
Need discharge <<2s



BU2

PROJECT : LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	1A

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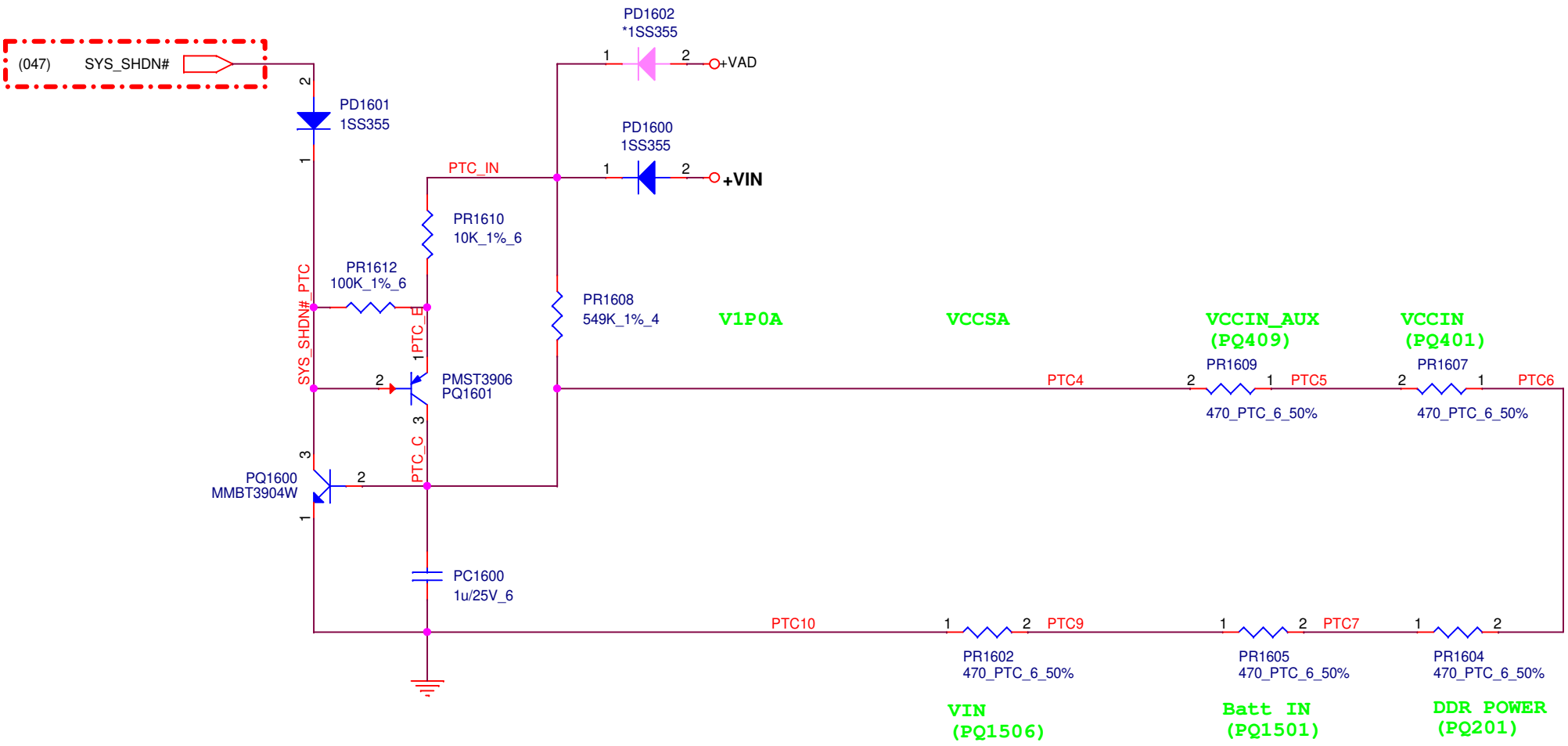

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BU2

PROJECT :LS2B

Quanta Computer Inc.

Size	Document Number	Rev
	PTC Circuit	1A

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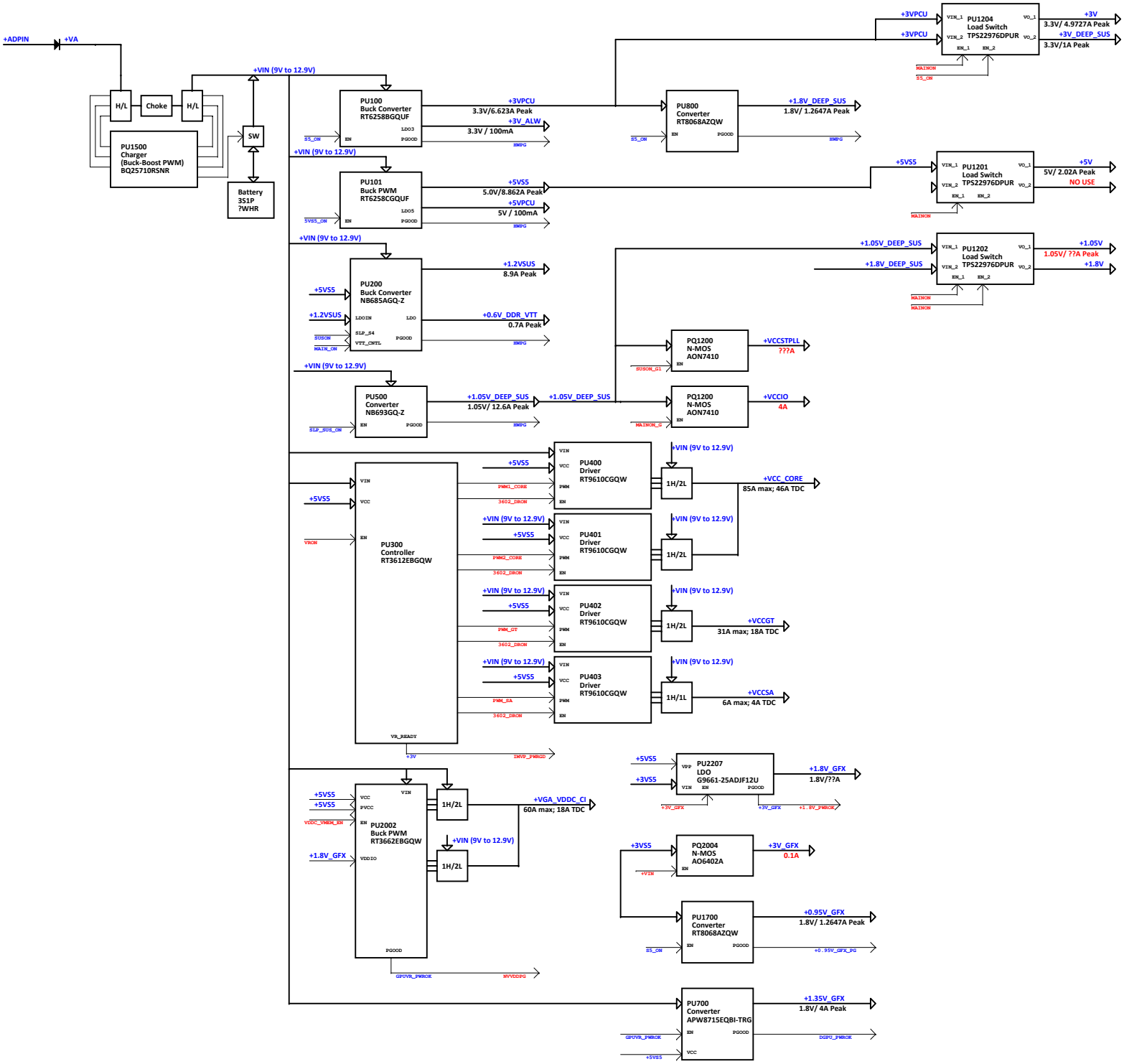
POWER BLOCK DIAGRAM



BU2	PROJECT : LS2B Quanta Computer Inc.	
	Size / Document Number: Power Map	Rev: 1A
	Date: Friday, September 25, 2020	Sheet 84 of 84